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<th>Author(s)</th>
<th>Supersedes</th>
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<td>4 May 2005</td>
<td>P. Young</td>
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Document Title
Limitations and Deviations for EGSE PDU Test Stand GLAT1164

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# CHANGE HISTORY LOG

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<td>Initial Release</td>
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# Limitations and Deviations for EGSE PDU Test Stand GLAT1164

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LAT-TD-06627-01
Limitations and Deviations for EGSE PDU Test Stand GLAT1164

1. **SCOPE**

This document lists

- Environmental limitations.
- Validation of this PDU Test Stand.

2. **ENVIRONMENTAL CONDITIONS**

- This PDU Test Stand is designed to operate at room temperature except for the cabling, some of which is placed in an environmental chamber.

3. **DIFFERENCES FROM RELEASED DRAWINGS**

3.1 **PDU Test Box**

- None.

4. **DEVIATIONS FROM TEST-PROCEDURES**

4.1 **LAT-TD-04095-01 (Validation Procedure)**

- Section 5.2.4, skipped (ATE Resistance Checks). The checks of this section validate the expected resistances of the test resistor boards that act as temperature sensor loads for the PDU under test. The PDU Performance Test (LAT-TD-01744) sufficiently validates these boards are safe and functional so the ATE Resistance Checks are not necessary.
- Section 5.3.5, performed on two cables, GLAT1647 and GLAT1200.
- Section 5.3.9, performed on two cables, GLAT1647 and GLAT1200.
- Section 5.3.11, completed Register Tests and Voltage Calibration Tests as required. However, only one Temperature Calibration Point Extraction performed (at the marginal operating condition called for in the procedure), without LAT-DS-05829 mux board. Second
Temperature Calibration Point Extraction performed at nominal operating conditions, with LAT-DS-05829 mux board. Results attached to data package. Note that the log files show that some RTDs fail the test. This is due to the additional resistance introduced by the mux board. The log files show how much these RTD measurements are off by. As of June 17, 2005, the software has been improved to account for the mux resistance with a lookup table based on the mux bank (1 of 8) being used.