<table>
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<tr>
<th>Document Title</th>
<th>Limitations and Deviations for TKR TEM Test-stand #5</th>
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<tr>
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<td>LAT-TD-03959-01</td>
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<td>Author(s)</td>
<td>Gunther Haller</td>
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<td>Subsystem/Office</td>
<td>Electronics &amp; DAQ Subsystem</td>
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## CHANGE HISTORY LOG

<table>
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<tr>
<th>Revision</th>
<th>Effective Date</th>
<th>Description of Changes</th>
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1. **SCOPE**

This document lists

- the environmental limitations and
- the differences of the test-stand shipped compared to the released test-stand drawings

2. **ENVIRONMENTAL CONDITION**

- The test-stand temperature must be held between 18C and 38C, so no thermal cycling is allowed.
- The test-stand was only tested at room-temperature.
- No vibration tests are allowed.
- The test-stand can not be operated in a vacuum chamber.

3. **DIFFERENCES TO RELEASE DRAWINGS**

3.1 **Tower Power Supply**

- LAT-DS-02388-01, CCA: No staking was applied, Item 17, 18 omitted.
- LAT-DS-02389-01, PWB, complete
- LAT-DS-02390-04, Schematic: Sheet 1 - R1,R2,R11,R12 not loaded; Sheet 2, VR5 not loaded. Other sheets: Capacitors added across TRK Power Switch changed from 0.1microF to 1.0microF. Changed D500 to 1N4489.
- LAT-DS-02391-04, Material list, complete
- LAT-DS-00995-06, LAT-DS-00995-04, TPS enclosure: Entire unit is electroless nickel plated. No hard anodized was used.
- LAT-DS-01482-03, TPS ASSEMBLY: NO component staking was applied (item 15 omitted); NO cable harness support was installed (item 16 omitted); Screw heads were not staked
Limitations and Deviations for TKR TEM Test-stand #5

- Assembly number was not marked on chassis

3.2 Tower Electronics Module

- LAT-DS-01650-02 - Schematic Diagram, TEM CCA
- LAT-TD-02230-01 - Bill of Materials, TEM CCA
  - For resistors R648, R649, R650, R651 instead of single 50 Ohm value, two 100 Ohm resistors in parallel are used. They loaded with one soldered on top of second resistor.
- LAT-DS-01646-04 - Circuit Card Assembly, TEM DAQ
  - Conformal coating not used
  - Component staking/potting not used
  - Screw heads not staked
- LAT-DS-01649-05 - Printed Wire Board, TEM
- LAT-DS-02583-01 - PWB Fab, Loading and Assembly
- LAT-DS-02588-02 - Connector and Cable Assembly, TEM CCA
- LAT-DS-00554-06 - TEM Box Base
  - Part is fully electroless nickel plated, no hard anodize was used
- LAT-DS-00555-06 - TEM Box Lid
  - Part is fully electroless nickel plated, no hard anodize was used
- LAT-DS-01481-04 - Assembly, Tower Electronics Module
  - Assy number not marked on chassis
- LAT-DS-01026-02 - TEM Connector Plate
- LAT-DS-01031-02 - TEM Connector Pin
- LAT-TD-01880-01 - VHDL, LAT TEM GTIC FPGA
- LAT-TD-01881-01 - VHDL, LAT TEM GTIU FPGA
- LAT-DS-03582-01 - Spacer, TEM Connector
FPGA version numbers:

- U45 – GTIC – version 1
- U62 – COMMCNTL version 1 (Preprogrammed firmware version 9)

4. **CHANGES FROM TEST-PROCEDURE**

The test-procedure was in the process of official LAT-DOC release while the tests were performed. No changes to the procedure were done between the executing the tests and official release of the procedure.

4.1 **Data Sheets and Cover Sheet**

The sheets used for recording all measurements were from the original draft document before it was approved and released.