LAT PROJECT DOCUMENT CHANGE NOTICE (DCN)

DCN No. LAT-XR-05546-01

SHEET 1 **OF** 1

ORIGINATOR: Leonid Sapozhnikov	**PHONE:** 650-926-2002	**DATE:** 1/7/05
CHANGE TITLE: DCN for TEM Specifications and Requirements Documents		**ORG.:**

DOCUMENT NUMBER	TITLE	NEW REV.
LAT-SS-05522	TEM Specification – Level V Specification	01
LAT-SS-05533	TEM/TPS Specification- Level V Specification	01
LAT-TD-05534	TEM Requirements Verification Matrix	01
LAT-TD-05536	TEM/TPS Requirements Verification Matrix	01

CHANGE DESCRIPTION (FROM/TO):

Initial release

REASON FOR CHANGE:

ACTION TAKEN: ☒ **Change(s) included in new release** ☐ **DCN attached to document(s), changes to be included in next revision**
☐ **Other (specify):**

DISPOSITION OF HARDWARE (IDENTIFY SERIAL NUMBERS):	**DCN DISTRIBUTION:**
☒ **No hardware affected (record change only)**	
☐ **List S/Ns which comply already:**	
☐ **List S/Ns to be reworked or scrapped:**	
☐ **List S/Ns to be built with this change:**	
☐ **List S/Ns to be retested per this change:**	
☐	

SAFETY, COST, SCHEDULE, REQUIREMENTS IMPACT? ☐ **YES** ☒ **NO**
If yes, CCB approval is required. Enter change request number:

APPROVALS	DATE	OTHER APPROVALS (specify):	DATE
ORIGINATOR: L. Sapozhnikov (signature on file)	1/7/05		
ORG. MANAGER: G. Haller (signature on file)	1/7/05		
PSA- Darren Marsh (signature on file)	1/7/05		
Manufacturing- R. Patterson (signature on file)	1/10/05		
Elec.- D. Nelson (signature on file)	1/7/05		
DCC RELEASE: Natalie Cramar (signature on file)	1/10/05	Doc. Control Level: ☒ Subsystem ☐ LAT IPO ☐ GLAST Project	

	Document #	Date effective
	**LAT-TD-05534-01**	01/05/2005
	Author(s) Leonid Sapozhnikov Philip Hart Jana Thayer	Supersedes
	Subsystem/Office Electronics & DAQ Subsystem	

Document Title

Tower Electronics Module (TEM) Requirements Verification Matrix

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
1	01/05/2005	Original release

Table of Contents -TOC

1. SCOPE

This document provides a matrix of the Tower Electronics Module (TEM) subsystem requirements to verification tests.

2. DEFINITIONS AND ACRONYMS

The following terms, abbreviations, and acronyms are used in this document:

2.1 Definitions

A, An	Analog
A	Analysis
D, Dg	Digital
DR	Data Rate
Eff	Efficiency
F	Functional
μs	microsecond
ns	nanosecond
P	Performance
P/F	Pass/Fail
V	Volt
W	Watt

2.2 Acronyms

AFEE	Analog Front End Electronics
AIDS	Assembly and Inspection Data Sheet
BOB	Break Out Box
BOC	Break Out Cable
CAL	Calorimeter
CC	Cable Controller
CSAM	Computer Scanning Acoustic Microscopy (computer sweeps the EUT with a tone to detect any voids in the ASIC)
EBM	Event Builder Module
EGSE	Electrical Ground Support Equipment
EICIT	Electrical Interface Continuity and Isolation Test (cold checks)
ETech	Electrical Technician
EUT	Equipment Under Test
FE	Front End
FIFO	First-in, First-Out

FPGA	Field-Programmable Gate Array
GASU	Global trigger, ACD, System Unit
GCCC	GLAST Calorimeter Cable Controller
GEM	Global-Trigger Electronics Module
GLAST	Gamma Ray Large Area Space Telescope
GTCC	GLAST Tracker Cable Controller
GTFE	GLAST Tracker Front End
GTRC	GLAST Tracker Readout Controller
HAST	Highly Accelerated Stress Test
ICD	Interface Control Document
LAT	Large Area Telescope
LATp	Large Area Telescope protocol
MCM	Multi Chip Module
MGSE	Mechanical Ground Support Equipment
STM	Safe To Mate
SVT	Stray Voltage Test (hot checks)
T&DF	Trigger and Data Flow
TACK	Trigger Acknowledge
TAM	Trigger Accept Message
TEM	Tower Electronics Module
TKR	Tracker
TPS	Tower Power Supply
TRG	Trigger

3. APPLICABLE DOCUMENTS

Reference	Document Number	Description
[1]	LAT-SS-00284	LAT Trigger Subsystems Specification – Level IV
[2]	LAT-SS-00285	LAT Dataflow Subsystems Specification – Level IV
[3]	LAT-TD-00605	TEM Programming ICD Specification
[4]	LAT-TD-00606	LAT Inter-Module Communications, Manual
[5]	LAT-SS-00183	Power Supply Modules Specification – Level IV
[6]	LAT-SS-00288	TEM Specification and ICD
[7]	GSFC 433-SPEC-0001	GLAST Mission System Specification
[8]	LAT-SS-00238	Calorimeter-LAT ICD
[9]	LAT-SS-00176	Tracker Electrical Interface Specification
[10]	LAT-SS-05522	Tower Electronics Module (TEM) Specification - Level V Specification
[11]	LAT-TD-03415	Tower Electronics Module Assembly Performance Test Procedure

4. TEM REQUIREMENTS TO TEST VERIFICATION MATRIX

For more information on the TEM requirements, see [9] and [10]. The Test Paragraph field below refers to the paragraph number in the Tower Electronics Module Assembly Test Procedure, [11]. Some requirements will be tested at System level, not at box level. This is indicated by the word "System" in the Test Paragraph field of the matrix.

Note: Verification methods are T = Test, A = Analysis, I = Inspection, S = Simulation

Table 1: TEM Requirements to Test Verification Matrix

Requirement Number	Title	Test Paragraph [11]	Verification Method
5.	DATAFLOW Requirements	NA	NA
5.1	General	NA	NA
5.1.1	LATp	5.4.4	Test
5.1.2	LATp Address	5.4.4	Test
5.1.3	Even/Odd Address	NA	NA
5.1.3.1	Even/Odd Address and Cabling	5.4.4/5.4.5/5.4.8	Test
5.1.3.2	Address independence	5.4.8	Test
5.1.4	Address Survives Resets	5.4.8	Test
5.1.5	Path Redundancy	5.4.4/5.4.8	Test
5.1.5.1	Path Indicator	5.4.8	Test
5.1.6	Communication to FEs	5.4.5	Test
5.1.7	Event Data Response	5.4.4	Test
5.1.8	Data Storage Guarantee	5.4.6/5.4.8	Test
5.1.8.1	Handling TKR Hit Data	5.4.6/5.4.8	Test
5.1.8.2	Handling Low Data Storage	5.4.6/5.4.8	Test
5.1.8.3	Transitory FIFO Signals	5.5.4.8	Test
5.1.8.4	Latched FIFO Signals	5.4.8	Test
5.1.9	Output Data Assembly	5.4.8	Test
5.1.10	LATp statistics	5.4.4	Test
5.1.10.1	Event Statistics	5.4.4/5.4.8	Test
5.1.10.2	Response Statistics	5.4.8	Test
5.1.10.3	Command Statistics	5.4.8	Test
5.1.11	Handling Failed Commands	5.4.8	Test
5.1.12	Serial Parity Generation	5.4.8	Test
5.1.13	Timing Out Cable Controllers	5.4.8	Test
5.1.14	CC Timeout Range	5.4.8	Test
5.1.15	Disabling CCs	5.4.8	Test
5.1.16	Diagnostic Mode	5.4.5/5.4.8	Test
5.1.17	Trigger Message in Event Data	5.4.4/5.4.8	Test
5.1.18	FPGA Version Number	5.4.8	Test

Requirement Number	Title	Test Paragraph [11]	Verification Method
5.1.19	Event Error Reporting	5.4.8	Test
5.1.20	Databus Protection	5.4.8	Test
5.1.20.1	CC Power-Up	5.4.8	Test
5.1.21	CC Trigger Primitive Alignment	5.4.8	Test
5.1.22	CC Trigger Primitive Alignment Range	5.4.8	Test
5.1.23	Trigger Jitter	System Level Test	Test
5.1.24	Trigger Round-Trip Alignment	5.4.6/System	Test
5.1.25	Trigger Round-Trip Delay Range	5.4.6/System	Test
5.2	Calorimeter Specific	NA	NA
5.2.1	CAL Cable Interface	5.4.6/5.4.8	Test
5.2.2	CAL Input Data Format	5.4.5/5.4.6/5.4.8	Test
5.2.3	Log-End Assembly	5.4.6/5.4.8	Test
5.2.4	Zero-Suppression	5.4.6/5.4.8	Test
5.2.4.1	Trigger Zero-Suppression Mode	5.4.8	Test
5.2.4.2	Log-End Accept Masking	5.4.8	Test
5.2.5	One-Or-Four-Range Readout	5.4.6/5.4.8	Test
5.2.6	Calibration Storage	5.4.6/5.4.8	Test
5.2.7	Deadtime Contribution	System	Test
5.2.8	Data Parity Error Reporting	5.4.8	Test
5.2.9	Data Coincidence and Timeout	5.4.8	Test
5.2.9	Timeout Setting	5.4.8	Test
5.2.10	First-Range Arrival Timeout	System	Test
5.2.11	Subsequent-Range Arrival Timeout	System	Test
5.3	Tracker Specific	NA	NA
5.3.1	TKR Cable Interface	5.4.5	Test
5.3.2	TKR Input Data Format	5.4.6	Test
5.3.3	Buffer Model Support	System	Test
5.3.4	Calibration Storage	5.4.6/5.4.8	Test
5.3.5	Cable Trimming	5.4.8	Test
5.3.6	TKR Event Data Mask	5.4.8	Test
5.3.7	Data Parity Error Reporting	5.4.8	Test
5.3.8	FE Error Support	5.4.8	Test
5.3.9	Tag Consistency Reporting	5.4.8	Test
5.3.10	Input Data Coincidence Reporting	5.4.8	Test
6.	TRIGGER	NA	NA
6.1	General	NA	NA
6.1.1	Trigger Configuration	5.4.6/5.4.8	Test
6.1.2	Trigger Accept Message	5.4.6/5.4.8	Test
6.1.3	TAM processing rate	System	Test

Requirement Number	Title	Test Paragraph [11]	Verification Method
6.1.4	Handling Low Data Storage, CAL	5.4.8	Test
6.1.5	Handling Low Data Storage, TKR	5.4.8	Test
6.1.6	TKR Trigger Signal Generation	5.4.4/5.4.8	Test
6.1.7	CALSTROBE Rate for TKR	System	Test
6.1.8	CAL Trigger Signal Generation	5.4.4/5.4.8	Test
6.1.9	CALSTROBE Rate for CAL	System	Test
6.1.10	CAL Zero Suppression Control	5.4.5/5.4.6/5.4.8	Test
6.1.11	Timing of Trigger Signals to TKR	5.4.8	Test
6.1.12	Timing of Trigger Signal to CAL	5.4.8	Test
6.1.13	CALSTROBE Timing	5.4.8/system	Test
6.1.14	CALSTROBE Timing	5.4.8	Test
6.1.15	Masking of Input Trigger Request Lines	5.4.5/5.4.8	Test
6.1.16	Separate CAL and TKR Deadtime Masking	5.4.8	Test
6.1.17	Stretch Time Setting	System	Test
6.2	Calorimeter Specific	NA	NA
6.2.1	CAL LO Inputs	5.4.5/5.4.8	Test
6.2.2	CAL LO Trigger Primitive	5.4.5/5.4.8	Test
6.2.3	CAL HI Inputs	5.4.5/5.4.8	Test
6.2.4	CAL HI Trigger Primitive	5.4.5/5.4.8	Test
6.2.5	Trigger Primitive Input Masking	5.4.5/5.4.8	Test
6.2.6	Trigger Latency	System	Test
6.3	Tracker Specific	NA	NA
6.3.1	TKR Trigger Inputs	5.4.5/5.4.8	Test
6.3.2	3-in-a-Row Trigger Primitive	5.4.5/5.4.8	Test
6.3.3	3-in-a-Row Input Masking	5.4.5/5.4.8	Test
6.3.4	3-in-a-Row Input Forced Assert	5.4.5/5.4.8	Test
6.3.5	Trigger Latency	System	Test
7.	POWER	NA	NA
7.1	Power Configuration	5.4.8	Test
7.2	Power Distribution	5.4.2/5.4.5/5.4.8	Test
7.3	FE power Supply Control, CAL	5.4.2/5.4.5/5.4.8	Test
7.4	FE power Supply Control, TKR	5.4.2/5.4.5/5.4.8	Test
7.5	Power-On Condition	5.4.8	Test
7.6	Power Setting Survives Reset	5.4.8	Test
7.7	High Voltage Setup	5.4.2	Test
8.	HOUSEKEEPING	NA	NA
8.1	Trigger statistics and dead-time counting	NA	NA
8.1.1	Deadtime Counting	5.4.8	Test
8.1.2	TKR Trigger Primitive Counting	5.4.5/.5.4.8	Test

Requirement Number	Title	Test Paragraph [11]	Verification Method
8.1.3	Masking for TKR Trigger Primitive Counting	5.4.8	Test
8.1.4	CAL Trigger Primitive Counting	5.4.5/5.4.8	Test
8.1.5	Masking for CAL Trigger Primitive Counting	5.4.5/5.4.8	Test
8.2	ENVIRONMENTAL MONITORING	NA	NA
8.2.1	Cable Temperature Measurement	5.4.2	Test
8.2.2	FE Voltage Measurement	5.4.2	Test
8.2.3	High Voltage Supply Current Measurement	5.4.2	Test
8.2.4	Tower Current Measurement	5.4.2	Test
8.2.5	Internal Voltage Measurement	5.4.2	Test
8.2.6	Signal Acquisition Indicator	System	Test
8.2.7	Temperature Sensors	5.4.3	Test
8.2.8	Redundant Voltage Sensors	5.4.2/System	Test