


Tower Electronics Module Assembly Test Procedure


COVER SHEET

Program: GLAST  
Procedure Number: LAT-TD-03415  
Procedure Title: TEM Performance Test Procedure  
Paragraph Number: 5.4  
Paragraph Title: Performance Tests  
Unit S/N: C12

TEST READINESS REVIEW COMPLETED AND APPROVED BY THE FOLLOWING:


Test Director: [Signature] Date: 12/14/04  
Quality Assurance: [Signature]  Date: 12/14/04  
Test Conductor: [Signature] Date: 12/14/04

REVIEWED AND APPROVED BY THE FOLLOWING:

Test Director: [Signature] Date: 12/15/04  
Quality Assurance: [Signature]  Date: 12/15/04  
Test Conductor: [Signature] Date: 12/15/04

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Tower Electronics Module Assembly Test Procedure



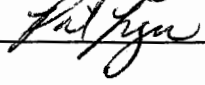
TEST DATA SHEET		Unit S/N: 612	Date/Temperature: 12/15/04/24.6°C
Title: 5.1.3 Test Equipment		Operator: C.S	QA: 
Para./ Step	Test Equipment Description, Manufacturer	Model/LAT Number	*Cal./Val. Date
5.1.3.1 - 1	Record Model/LAT number, Serial/Revision number, Calibration due dates and Validation date for all equipment used in this procedure:		
	VME Crate, Dawn VME Products	11-1011777-2119 VME64x (series 767)	CLAT1132
	VME, TST-STP Trans card	LAT-DS-00999	CLAT0216
	VME SBC MVME2304 card, Motorola	PN MVME2304-0123	CLAT0305
	VME LCB Mezzanine card	LAT-TD-00860	CLAT0822
	Software for the local PC	LATTE P04-04-01 <a href="http://www-glast.slac.stanford.edu/IntegrationTest/ONLINE/updates/">www-glast.slac.stanford.edu/IntegrationTest/ONLINE/updates/</a>	OK
	Software for the local PC	TEMPROD V00-00-00	OK
	DC Power supply #1, BK Precision	1697	CLAT1485
	DC Power supply #2, BK Precision	1697	CLAT1336
	28 Volt supply cable	LAT-DS-03246	N/A
	PS Control cable	LAT-DS-04831	CLAT1420
	TEM to GASU cable	LAT-DS-02106	CLAT1471
	LCB Transition board cable	LAT-DS-03247	CLAT1314
	TEM Test Board Assembly	LAT-DS-04465	CLAT0477
	TEM Test board cooling fan assembly	LAT-DS-03567	CLAT0022
	CAT5 Ethernet cable	TRD855PL-50	N/A
	RS-232 Cable	TDC003-7 (RECO98M connectors)	N/A
	Ground jumper, Banana, Pomona	B-12-0	N/A
	PS extension cable	LAT-DS-04629	CLAT1397
	Digital Multimeter, Fluke/Meterman	87-III/38XR	SCAC00004

\* This column is used to enter the date that equipment is validated, when validated equipment is recorded in this data sheet.

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All test setup validated on 12/15/04

Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N: 612	Date/Temperature: 12/15/04/ambient
Title: 5.1.4 Participant List		Operator: C.S.	QA: 
Para./ Step	Title	Print Name	Signature
5.1.4 - 1	<b>Record names of all personnel that take part in the test/operation:</b>		
	elect. eng	L. SADOHNIKA	
	PA QE	PAT LUTON	


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Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N: <i>612</i>	Date: <i>12/15/09</i>	
Title: 5.3 Pre Operation Verifications		Operator: <i>C-S</i>	QA: 	
Step	Description	Requirement	Units	Data
5.3	<b>Pre-Operation Verifications</b>			
-1	Notify QAE.	OK	OK/NG	<i>OK</i>
-2	Test Readiness Review is done.	OK	OK/NG	<i>OK</i>
-3	Record the EUT equipment:			
	TEM Part number	NA	NA	<i>LAT-DS-04640-5A</i>
	TEM LAT Bay location	NA	NA	<i>N/A</i>
	TEM Serial number	NA	NA	<i>612</i>
	TPS Part number	NA	NA	<i>CLAT0386</i>
	TPS LAT Bay location	NA	NA	<i>N/A</i>
	TPS Serial number	NA	NA	<i>N/A</i>
-4	Power on the LAT or EGSE is off.	OFF	ON/OFF	<i>OFF</i>
-5	Set DMM to autoranging for resistance.	OK	OK/NG	<i>OK</i>
-6	Measure DMM lead resistance.	<2.0	Ω	<i>0.2</i>
-7	Measure EUT to ground.	<2.0	Ω	<i>0.5</i>
-8	Measure equipment to ground.	<2.0	Ω	<i>0.6</i>
-9	All connector savers are installed on the flight connections.	OK	OK/NG	<i>OK</i>
-10	The test equipment and participant lists have been completed.	OK	OK/NG	<i>OK</i>

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## Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N: <div style="text-align: center; font-size: 1.2em;">612</div>	Date/Temperature: <div style="text-align: center; font-size: 1.2em;">12/15/04</div>		
Paragraph: 5.4 Performance Tests		Operator: <div style="text-align: center; font-size: 1.2em;">C.S</div>	QA: 		
Step	Description	Requirement	Units	Data	
<b>5.4.2 Monitor Margin and Bias Test Procedure</b>					
-11	Verify all tests passed by green indicators and no errors in the Messages box on the Margin and Bias Test window.	OK	OK/NG	OK*	
-12	Attach printout of the Monitor Margin and Bias Test log file to this data package.	OK	OK/NG	OK	
<b>5.4.3 Temperature Monitor Test</b>					
-11	Verify the test passed by green indicator and no errors in the Messages box on the Temperature Tests window.	OK	OK/NG	OK	
-12	Attach printout of the Temperature Monitor Test log file to this data package.	OK	OK/NG	OK	
<b>5.4.4 Basic Test</b>					
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG	OK	
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG	OK	
<b>5.4.5 Front End Test</b>					
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG	OK	
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG	OK	
<b>5.4.6 TEM FIFO Test</b>					
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG	OK	
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG	OK	

Midrange 0.001 - 0.005 A  
 High range 0.003 - 0.005 A  
 Range for TRK Bias current is

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Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.1 Multiple Frequency Test at +55° C		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.2	Monitor Margin and Bias Test				
-11	Verify test passed by green indicator and no errors in the Messages box on the Margin and Bias Test window.	OK	OK/NG		
-12	Attach printout of the Monitor Margin and Bias Test log file to this data package.	OK	OK/NG		

N/A

Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:	
Paragraph: 5.4.7.1 Multiple Frequency Test at +55° C (23 MHz)		Operator:	QA:	
Step	Description	Requirement	Units	Data
5.4.4	Basic Test			
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG	
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG	
5.4.5	Front End Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG	
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG	
5.4.6	FIFO Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG	
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG	

✓ N/A

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Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:	
Paragraph: 5.4.7.1 Multiple Frequency Test at +55° C (14 MHz)		Operator:	QA:	
Step	Description	Requirement	Units	Data
5.4.4	Basic Test			
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG	
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG	
5.4.5	Front End Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG	
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG	
5.4.6	FIFO Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG	
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG	

V  
N/A

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Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.1 Multiple Frequency Test at +55° C (20 MHz)		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.4	Basic Test				
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG		
5.4.5	Front End Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG		
5.4.6	FIFO Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG		
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG		

↓  
N/A

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Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.2 Multiple Frequency Test at -40° C		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.2	Monitor Margin and Bias Test				
-11	Verify test passed by green indicator and no errors in the Messages box on the Margin and Bias Test window.	OK	OK/NG		
-12	Attach printout of the Monitor Margin and Bias Test log file to this data package.	OK	OK/NG		

N/A

## Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.2 Multiple Frequency Test at 40° C (23 MHz)		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.4	Basic Test				
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG		
5.4.5	Front End Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG		
5.4.6	FIFO Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG		
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG		

N/A

Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.2 Multiple Frequency Test at -40° C (14 MHz)		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.4	Basic Test				
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG		
5.4.5	Front End Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG		
5.4.6	FIFO Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG		
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG		

N/A

## Tower Electronics Module Assembly Test Procedure

TEST DATA SHEET		Unit S/N:	Date/Temperature:		
Paragraph: 5.4.7.2 Multiple Frequency Test at -40° C (20 MHz)		Operator:	QA:		
Step	Description	Requirement	Units	Data	
5.4.4	Basic Test				
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG		
5.4.5	Front End Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG		
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG		
5.4.6	FIFO Test				
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG		
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG		

N/A

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Tower Electronics Module Assembly Test Procedure

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TEST DATA SHEET		Unit S/N: <i>612</i>	Date/Temperature: <i>12/15/04 / 64.610K</i>	
Paragraph: 5.4.8 Functional Test Procedure		Operator: <i>L.S</i>	QA:	
Step	Description	Requirement	Units	Data
5.4.8	Functional Test			
-8	Verify all tests passed by green indicators and no errors in the Messages box on the Functional Test window.	OK	OK/NG	<i>OK</i>
-9	Attach printout of the Functional Test log file to this data package.	OK	OK/NG	<i>OK</i>

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bias\_0386\_612\_20041215\_110057

11:00:57 no input file used for cal in this mode; use default slope 1.000000 and  
intercept 0.000000  
11:00:57 no input file used for tkr in this mode; use default slope 1.000000 and  
intercept 0.000000  
11:00:57 reading input file  
V:\GLAST\Electronics\TEMPROD\TpsCalibTest\data\tps\_0386\_612\_20041215\_105942.csv  
11:00:57 using slope 65.658863 and intercept -0.122454  
11:01:02

--- Testing Low Range ---

11:01:02 Pdu TEM voltage 0: Raw 2351 Calibrated 2.870 v: tolerance 2.7-3.0 v  
result: ok  
11:01:02 Pdu TEM voltage 1: Raw 2352 Calibrated 2.871 v: tolerance 2.7-3.0 v  
result: ok  
11:01:02 TEM : Raw 2352 Calibrated 2.871 v: tolerance 2.7-3.0 v  
result: ok  
11:01:02 Cal Digital : Raw 2318 Calibrated 2.830 v: tolerance 2.7-3.0 v  
result: ok  
11:01:02 Cal Analog : Raw 2360 Calibrated 2.881 v: tolerance 2.7-3.0 v  
result: ok  
11:01:02 Tkr Digital : Raw 2254 Calibrated 2.064 v: tolerance 2.0-2.2 v  
result: ok  
11:01:02 Tkr Analog A : Raw 1426 Calibrated 1.093 v: tolerance 1.0-1.35 v  
result: ok  
11:01:02 Tkr Analog B : Raw 2295 Calibrated 2.101 v: tolerance 1.9-2.3 v  
result: ok  
11:01:02 Cal Bias 1 : Raw 418 Calibrated 25.83 v: tolerance 24.0-27.0  
V result: ok  
11:01:02 Cal Bias 0 : Raw 18 Calibrated 1.111 v: tolerance 0.0-1.999  
V result: ok  
11:01:02 Cal Bias Current : Calibrated 0.004847 A: tolerance  
0.004-0.006 A result: ok  
11:01:02 Tkr Bias 1 : Raw 418 Calibrated 25.82 v: tolerance 24.0-27.0  
V result: ok  
11:01:02 Tkr Bias 0 : Raw 17 Calibrated 1.048 v: tolerance 0.0-2.0 v  
result: ok  
11:01:02 Tkr Bias Current : Calibrated 0.004858 A: tolerance  
0.004-0.006 A result: ok  
11:01:02 Tower 28V V1 : Raw 3396 Calibrated 27.41 v: tolerance 26.0-28.0  
V result: ok  
11:01:02 Tower 28V V2 : Raw 3417 Calibrated 27.58 v: tolerance 26.0-28.0  
V result: ok  
11:01:02 Current Calculation:  $I=65.659*(2.5/4095)*(V2-V1)+-0.122$   
11:01:02 Tower Current : Calibrated 0.73876 A: tolerance 0.6-0.9 A  
result: ok  
11:01:06

--- Testing High Range ---

11:01:06 Pdu TEM voltage 0: Raw 2919 Calibrated 3.564 v: tolerance 3.5-3.7 v  
result: ok  
11:01:06 Pdu TEM voltage 1: Raw 2913 Calibrated 3.556 v: tolerance 3.5-3.7 v  
result: ok  
11:01:06 TEM : Raw 2908 Calibrated 3.550 v: tolerance 3.5-3.7 v  
result: ok  
11:01:06 Cal Digital : Raw 3030 Calibrated 3.699 v: tolerance 3.6-4.0 v  
result: ok  
11:01:06 Cal Analog : Raw 3083 Calibrated 3.764 v: tolerance 3.6-4.0 v  
result: ok  
11:01:06 Tkr Digital : Raw 3202 Calibrated 2.932 v: tolerance 2.9-3.1 v  
result: ok  
11:01:06 Tkr Analog A : Raw 2117 Calibrated 1.622 v: tolerance 1.6-1.8 v

bias\_0386\_612\_20041215\_110057

result: ok  
 11:01:06 Tkr Analog B : Raw 3256 Calibrated 2.981 v: tolerance 2.85-3.1 v  
 result: ok  
 11:01:06 Cal Bias 1 : Raw 1672 Calibrated 103.1 v: tolerance 80.0-110.0  
 V result: ok  
 11:01:06 Cal Bias 0 : Raw 1545 Calibrated 95.30 v: tolerance 70.0-100.0  
 V result: ok  
 11:01:06 Cal Bias Current : Calibrated 0.001529 A: tolerance  
 0.001-0.002 A result: ok  
 11:01:06 Tkr Bias 1 : Raw 2570 Calibrated 158.5 v: tolerance  
 145.0-165.0 V result: ok  
 11:01:06 Tkr Bias 0 : Raw 2232 Calibrated 137.6 v: tolerance  
 130.0-150.0 V result: ok  
 11:01:06 Tkr Bias Current is 0.004092 for High test: out of tolerance range *Range 0.003-0.004*  
 0.003000-0.004000  
 11:01:06 Tkr Bias Current : Calibrated 0.004091 A: tolerance  
 0.003-0.004 A result: high  
 11:01:06 Tower 28V V1 : Raw 3343 Calibrated 26.98 v: tolerance 26.0-28.0  
 V result: ok  
 11:01:06 Tower 28V V2 : Raw 3379 Calibrated 27.27 v: tolerance 26.0-28.0  
 V result: ok  
 11:01:06 Current Calculation:  $I=65.659*(2.5/4095)*(V2-V1)+-0.122$   
 11:01:06 Tower Current : Calibrated 1.32921 A: tolerance 1.1-1.5 A  
 result: ok  
 11:01:11

--- Testing MidRange Range ---

11:01:11 Pdu TEM voltage 0: Raw 2726 Calibrated 3.328 v: tolerance 3.25-3.45  
 V result: ok  
 11:01:11 Pdu TEM voltage 1: Raw 2729 Calibrated 3.332 v: tolerance 3.25-3.45  
 V result: ok  
 11:01:11 TEM : Raw 2722 Calibrated 3.323 v: tolerance 3.25-3.45  
 V result: ok  
 11:01:11 Cal Digital : Raw 2679 Calibrated 3.271 v: tolerance 3.25-3.45  
 V result: ok  
 11:01:11 Cal Analog : Raw 2726 Calibrated 3.328 v: tolerance 3.25-3.45  
 V result: ok  
 11:01:11 Tkr Digital : Raw 2733 Calibrated 2.502 v: tolerance 2.5-2.7 v  
 result: ok  
 11:01:11 Tkr Analog A : Raw 1772 Calibrated 1.358 v: tolerance 1.3-1.6 v  
 result: ok  
 11:01:11 Tkr Analog B : Raw 2783 Calibrated 2.548 v: tolerance 2.35-2.73  
 V result: ok  
 11:01:11 Cal Bias 1 : Raw 876 Calibrated 54.02 v: tolerance 45.0-55.0  
 V result: ok  
 11:01:11 Cal Bias 0 : Raw 820 Calibrated 50.56 v: tolerance 40.0-55.0  
 V result: ok  
 11:01:11 Cal Bias Current : Calibrated 0.000679 A: tolerance  
 0.0005-0.001 A result: ok  
 11:01:11 Tkr Bias 1 : Raw 1289 Calibrated 79.51 v: tolerance 70.0-85.0  
 V result: ok  
 11:01:11 Tkr Bias 0 : Raw 1120 Calibrated 69.11 v: tolerance 60.0-75.0  
 V result: ok  
 11:01:11 Tkr Bias Current is 0.002040 for MidRange test: out of tolerance range *Range 0.001-0.002*  
 0.001000-0.002000  
 11:01:11 Tkr Bias Current : Calibrated 0.002040 A: tolerance  
 0.001-0.002 A result: high  
 11:01:11 Tower 28V V1 : Raw 3372 Calibrated 27.21 v: tolerance 26.0-28.0  
 V result: ok  
 11:01:11 Tower 28V V2 : Raw 3400 Calibrated 27.44 v: tolerance 26.0-28.0  
 V result: ok  
 11:01:11 Current Calculation:  $I=65.659*(2.5/4095)*(V2-V1)+-0.122$



11:01:11 Tower Current  
result: ok

bias\_0386\_612\_20041215\_110057  
: Calibrated 0.99651 A: tolerance 0.9-1.3 A

## temp\_0386\_612\_20041215\_110255

11:02:56 Cal 0 T0: Raw 3157 Calibrated 27.5 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 0 T1: Raw 3174 Calibrated 28.2 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 1 T0: Raw 3144 Calibrated 27.0 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 1 T1: Raw 3168 Calibrated 28.0 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 2 T0: Raw 3139 Calibrated 26.8 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 2 T1: Raw 3160 Calibrated 27.6 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 3 T0: Raw 3145 Calibrated 27.1 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Cal 3 T1: Raw 3190 Calibrated 28.8 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 0 T0: Raw 3178 Calibrated 28.4 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 0 T1: Raw 3161 Calibrated 27.7 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 1 T0: Raw 3152 Calibrated 27.3 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 1 T1: Raw 3185 Calibrated 28.6 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 2 T0: Raw 3183 Calibrated 28.6 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 2 T1: Raw 3230 Calibrated 30.5 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 3 T0: Raw 3144 Calibrated 27.0 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 3 T1: Raw 3173 Calibrated 28.2 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 4 T0: Raw 3142 Calibrated 26.9 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 4 T1: Raw 3187 Calibrated 28.7 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 5 T0: Raw 3131 Calibrated 26.5 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 5 T1: Raw 3156 Calibrated 27.5 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 6 T0: Raw 3172 Calibrated 28.1 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 6 T1: Raw 3138 Calibrated 26.8 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 7 T0: Raw 3156 Calibrated 27.5 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tkr 7 T1: Raw 3195 Calibrated 29.0 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 PS T0 : Raw 3125 Calibrated 26.3 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 PS T1 : Raw 3106 Calibrated 25.6 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tem T0 : Raw 3123 Calibrated 26.2 C tolerance range 20.0-35.0C  
result: ok  
11:02:56 Tem T1 : Raw 3116 Calibrated 26.0 C tolerance range 20.0-35.0C  
result: ok

basic\_20041215\_110312

12/15/04 11:03:55 INFO Test Over: All tests Successful

temFe\_20041215\_110406

12/15/04	11:04:15	INFO	GTCC 0 - Analog A	Ref: 1.360 V	Actual: 1.284 V
12/15/04	11:04:15	INFO	GTCC 0 - Analog B	Ref: 2.553 V	Actual: 2.539 V
12/15/04	11:04:15	INFO	GTCC 0 - Digital	Ref: 2.506 V	Actual: 2.439 V
12/15/04	11:04:15	INFO	GTCC 0 - High Voltage	Ref: 136.5 V	Actual: 135.7 V
12/15/04	11:04:15	INFO	GTCC 0 - High Voltage by 2		Actual: 50.31 V
12/15/04	11:04:15	INFO	GTCC 1 - Analog A	Ref: 1.360 V	Actual: 1.294 V
12/15/04	11:04:15	INFO	GTCC 1 - Analog B	Ref: 2.553 V	Actual: 2.544 V
12/15/04	11:04:15	INFO	GTCC 1 - Digital	Ref: 2.506 V	Actual: 2.451 V
12/15/04	11:04:15	INFO	GTCC 1 - High Voltage	Ref: 136.5 V	Actual: 135.4 V
12/15/04	11:04:15	INFO	GTCC 1 - High Voltage by 2		Actual: 48.83 V
12/15/04	11:04:15	INFO	GTCC 2 - Analog A	Ref: 1.360 V	Actual: 1.293 V
12/15/04	11:04:15	INFO	GTCC 2 - Analog B	Ref: 2.553 V	Actual: 2.539 V
12/15/04	11:04:15	INFO	GTCC 2 - Digital	Ref: 2.506 V	Actual: 2.446 V
12/15/04	11:04:15	INFO	GTCC 2 - High Voltage	Ref: 136.5 V	Actual: 135.7 V
12/15/04	11:04:15	INFO	GTCC 2 - High Voltage by 2		Actual: 49.82 V
12/15/04	11:04:15	INFO	GTCC 3 - Analog A	Ref: 1.360 V	Actual: 1.308 V
12/15/04	11:04:15	INFO	GTCC 3 - Analog B	Ref: 2.553 V	Actual: 2.542 V
12/15/04	11:04:15	INFO	GTCC 3 - Digital	Ref: 2.506 V	Actual: 2.456 V
12/15/04	11:04:15	INFO	GTCC 3 - High Voltage	Ref: 136.5 V	Actual: 135.6 V
12/15/04	11:04:15	INFO	GTCC 3 - High Voltage by 2		Actual: 53.08 V
12/15/04	11:04:15	INFO	GTCC 4 - Analog A	Ref: 1.360 V	Actual: 1.316 V
12/15/04	11:04:15	INFO	GTCC 4 - Analog B	Ref: 2.553 V	Actual: 2.544 V
12/15/04	11:04:15	INFO	GTCC 4 - Digital	Ref: 2.506 V	Actual: 2.481 V
12/15/04	11:04:15	INFO	GTCC 4 - High Voltage	Ref: 136.5 V	Actual: 135.5 V
12/15/04	11:04:15	INFO	GTCC 4 - High Voltage by 2		Actual: 51.30 V
12/15/04	11:04:15	INFO	GTCC 5 - Analog A	Ref: 1.360 V	Actual: 1.324 V
12/15/04	11:04:15	INFO	GTCC 5 - Analog B	Ref: 2.553 V	Actual: 2.554 V
12/15/04	11:04:15	INFO	GTCC 5 - Digital	Ref: 2.506 V	Actual: 2.483 V
12/15/04	11:04:15	INFO	GTCC 5 - High Voltage	Ref: 136.5 V	Actual: 135.2 V
12/15/04	11:04:15	INFO	GTCC 5 - High Voltage by 2		Actual: 48.77 V
12/15/04	11:04:15	INFO	GTCC 6 - Analog A	Ref: 1.360 V	Actual: 1.326 V
12/15/04	11:04:15	INFO	GTCC 6 - Analog B	Ref: 2.553 V	Actual: 2.555 V
12/15/04	11:04:15	INFO	GTCC 6 - Digital	Ref: 2.506 V	Actual: 2.481 V
12/15/04	11:04:15	INFO	GTCC 6 - High Voltage	Ref: 136.5 V	Actual: 137.8 V
12/15/04	11:04:15	INFO	GTCC 6 - High Voltage by 2		Actual: 48.58 V
12/15/04	11:04:15	INFO	GTCC 7 - Analog A	Ref: 1.360 V	Actual: 1.319 V
12/15/04	11:04:15	INFO	GTCC 7 - Analog B	Ref: 2.553 V	Actual: 2.554 V
12/15/04	11:04:15	INFO	GTCC 7 - Digital	Ref: 2.506 V	Actual: 2.481 V
12/15/04	11:04:15	INFO	GTCC 7 - High Voltage	Ref: 136.5 V	Actual: 134.6 V
12/15/04	11:04:15	INFO	GTCC 7 - High Voltage by 2		Actual: 49.14 V
12/15/04	11:04:21	INFO	GCCC 0 - Analog	Ref: 3.335 V	Actual: 3.194 V
12/15/04	11:04:21	INFO	GCCC 0 - Digital	Ref: 3.278 V	Actual: 3.091 V
12/15/04	11:04:21	INFO	GCCC 0 - High Voltage	Ref: 39.27 V	Actual: 40.57 V
12/15/04	11:04:21	INFO	GCCC 1 - Analog	Ref: 3.335 V	Actual: 3.216 V
12/15/04	11:04:21	INFO	GCCC 1 - Digital	Ref: 3.278 V	Actual: 3.145 V
12/15/04	11:04:21	INFO	GCCC 1 - High Voltage	Ref: 39.27 V	Actual: 40.51 V
12/15/04	11:04:21	INFO	GCCC 2 - Analog	Ref: 3.335 V	Actual: 3.196 V
12/15/04	11:04:21	INFO	GCCC 2 - Digital	Ref: 3.278 V	Actual: 3.140 V
12/15/04	11:04:21	INFO	GCCC 2 - High Voltage	Ref: 39.27 V	Actual: 40.26 V
12/15/04	11:04:21	INFO	GCCC 3 - Analog	Ref: 3.335 V	Actual: 3.194 V
12/15/04	11:04:21	INFO	GCCC 3 - Digital	Ref: 3.278 V	Actual: 3.174 V
12/15/04	11:04:21	INFO	GCCC 3 - High Voltage	Ref: 39.27 V	Actual: 40.44 V

## temFe\_20041215\_110406

12/15/04	11:04:29	INFO	GTCC 0 - Analog A	Ref: 1.358 V	Actual: 1.280 V
12/15/04	11:04:29	INFO	GTCC 0 - Analog B	Ref: 2.549 V	Actual: 2.536 V
12/15/04	11:04:30	INFO	GTCC 0 - Digital	Ref: 2.503 V	Actual: 2.437 V
12/15/04	11:04:30	INFO	GTCC 0 - High Voltage	Ref: 137.9 V	Actual: 137.1 V
12/15/04	11:04:30	INFO	GTCC 0 - High Voltage by 2		Actual: 50.74 V
12/15/04	11:04:30	INFO	GTCC 1 - Analog A	Ref: 1.358 V	Actual: 1.290 V
12/15/04	11:04:30	INFO	GTCC 1 - Analog B	Ref: 2.549 V	Actual: 2.542 V
12/15/04	11:04:30	INFO	GTCC 1 - Digital	Ref: 2.503 V	Actual: 2.449 V
12/15/04	11:04:30	INFO	GTCC 1 - High Voltage	Ref: 137.9 V	Actual: 136.8 V
12/15/04	11:04:30	INFO	GTCC 1 - High Voltage by 2		Actual: 49.32 V
12/15/04	11:04:30	INFO	GTCC 2 - Analog A	Ref: 1.358 V	Actual: 1.290 V
12/15/04	11:04:30	INFO	GTCC 2 - Analog B	Ref: 2.549 V	Actual: 2.536 V
12/15/04	11:04:30	INFO	GTCC 2 - Digital	Ref: 2.503 V	Actual: 2.443 V
12/15/04	11:04:30	INFO	GTCC 2 - High Voltage	Ref: 137.9 V	Actual: 137.1 V
12/15/04	11:04:30	INFO	GTCC 2 - High Voltage by 2		Actual: 50.19 V
12/15/04	11:04:30	INFO	GTCC 3 - Analog A	Ref: 1.358 V	Actual: 1.306 V
12/15/04	11:04:30	INFO	GTCC 3 - Analog B	Ref: 2.549 V	Actual: 2.539 V
12/15/04	11:04:30	INFO	GTCC 3 - Digital	Ref: 2.503 V	Actual: 2.454 V
12/15/04	11:04:30	INFO	GTCC 3 - High Voltage	Ref: 137.9 V	Actual: 137.1 V
12/15/04	11:04:30	INFO	GTCC 3 - High Voltage by 2		Actual: 53.76 V
12/15/04	11:04:30	INFO	GTCC 4 - Analog A	Ref: 1.358 V	Actual: 1.312 V
12/15/04	11:04:30	INFO	GTCC 4 - Analog B	Ref: 2.549 V	Actual: 2.543 V
12/15/04	11:04:30	INFO	GTCC 4 - Digital	Ref: 2.503 V	Actual: 2.477 V
12/15/04	11:04:30	INFO	GTCC 4 - High Voltage	Ref: 137.9 V	Actual: 136.9 V
12/15/04	11:04:30	INFO	GTCC 4 - High voltage by 2		Actual: 51.79 V
12/15/04	11:04:30	INFO	GTCC 5 - Analog A	Ref: 1.358 V	Actual: 1.323 V
12/15/04	11:04:30	INFO	GTCC 5 - Analog B	Ref: 2.549 V	Actual: 2.551 V
12/15/04	11:04:30	INFO	GTCC 5 - Digital	Ref: 2.503 V	Actual: 2.481 V
12/15/04	11:04:30	INFO	GTCC 5 - High Voltage	Ref: 137.9 V	Actual: 136.7 V
12/15/04	11:04:30	INFO	GTCC 5 - High Voltage by 2		Actual: 49.26 V
12/15/04	11:04:30	INFO	GTCC 6 - Analog A	Ref: 1.358 V	Actual: 1.323 V
12/15/04	11:04:30	INFO	GTCC 6 - Analog B	Ref: 2.549 V	Actual: 2.554 V
12/15/04	11:04:30	INFO	GTCC 6 - Digital	Ref: 2.503 V	Actual: 2.477 V
12/15/04	11:04:30	INFO	GTCC 6 - High Voltage	Ref: 137.9 V	Actual: 139.3 V
12/15/04	11:04:30	INFO	GTCC 6 - High Voltage by 2		Actual: 49.02 V
12/15/04	11:04:30	INFO	GTCC 7 - Analog A	Ref: 1.358 V	Actual: 1.318 V
12/15/04	11:04:30	INFO	GTCC 7 - Analog B	Ref: 2.549 V	Actual: 2.551 V
12/15/04	11:04:30	INFO	GTCC 7 - Digital	Ref: 2.503 V	Actual: 2.478 V
12/15/04	11:04:30	INFO	GTCC 7 - High Voltage	Ref: 137.9 V	Actual: 136.1 V
12/15/04	11:04:30	INFO	GTCC 7 - High Voltage by 2		Actual: 49.69 V
12/15/04	11:04:35	INFO	GCCC 0 - Analog	Ref: 3.330 V	Actual: 3.194 V
12/15/04	11:04:35	INFO	GCCC 0 - Digital	Ref: 3.274 V	Actual: 3.091 V
12/15/04	11:04:35	INFO	GCCC 0 - High Voltage	Ref: 95.69 V	Actual: 98.16 V
12/15/04	11:04:35	INFO	GCCC 1 - Analog	Ref: 3.330 V	Actual: 3.213 V
12/15/04	11:04:35	INFO	GCCC 1 - Digital	Ref: 3.274 V	Actual: 3.145 V
12/15/04	11:04:35	INFO	GCCC 1 - High Voltage	Ref: 95.69 V	Actual: 97.17 V
12/15/04	11:04:35	INFO	GCCC 2 - Analog	Ref: 3.330 V	Actual: 3.194 V
12/15/04	11:04:35	INFO	GCCC 2 - Digital	Ref: 3.274 V	Actual: 3.137 V
12/15/04	11:04:35	INFO	GCCC 2 - High Voltage	Ref: 95.69 V	Actual: 95.94 V
12/15/04	11:04:35	INFO	GCCC 3 - Analog	Ref: 3.330 V	Actual: 3.189 V
12/15/04	11:04:35	INFO	GCCC 3 - Digital	Ref: 3.274 V	Actual: 3.174 V

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12/15/04	11:04:35	INFO	GCCC 3 - High Voltage	Ref: 95.69 V	Actual: 95.32 V
12/15/04	11:04:44	INFO	GTCC 0 - Analog A	Ref: 1.357 V	Actual: 1.280 V
12/15/04	11:04:44	INFO	GTCC 0 - Analog B	Ref: 2.549 V	Actual: 2.536 V
12/15/04	11:04:44	INFO	GTCC 0 - Digital	Ref: 2.502 V	Actual: 2.437 V
12/15/04	11:04:44	INFO	GTCC 0 - High Voltage	Ref: 137.9 V	Actual: 137.1 V
12/15/04	11:04:44	INFO	GTCC 0 - High Voltage by 2		Actual: 50.80 V
12/15/04	11:04:44	INFO	GTCC 1 - Analog A	Ref: 1.357 V	Actual: 1.290 V
12/15/04	11:04:44	INFO	GTCC 1 - Analog B	Ref: 2.549 V	Actual: 2.542 V
12/15/04	11:04:44	INFO	GTCC 1 - Digital	Ref: 2.502 V	Actual: 2.449 V
12/15/04	11:04:44	INFO	GTCC 1 - High Voltage	Ref: 137.9 V	Actual: 136.9 V
12/15/04	11:04:44	INFO	GTCC 1 - High Voltage by 2		Actual: 49.32 V
12/15/04	11:04:44	INFO	GTCC 2 - Analog A	Ref: 1.357 V	Actual: 1.290 V
12/15/04	11:04:44	INFO	GTCC 2 - Analog B	Ref: 2.549 V	Actual: 2.536 V
12/15/04	11:04:44	INFO	GTCC 2 - Digital	Ref: 2.502 V	Actual: 2.443 V
12/15/04	11:04:44	INFO	GTCC 2 - High Voltage	Ref: 137.9 V	Actual: 137.2 V
12/15/04	11:04:44	INFO	GTCC 2 - High Voltage by 2		Actual: 50.25 V
12/15/04	11:04:44	INFO	GTCC 3 - Analog A	Ref: 1.357 V	Actual: 1.306 V
12/15/04	11:04:44	INFO	GTCC 3 - Analog B	Ref: 2.549 V	Actual: 2.539 V
12/15/04	11:04:44	INFO	GTCC 3 - Digital	Ref: 2.502 V	Actual: 2.454 V
12/15/04	11:04:44	INFO	GTCC 3 - High Voltage	Ref: 137.9 V	Actual: 137.1 V
12/15/04	11:04:44	INFO	GTCC 3 - High Voltage by 2		Actual: 53.76 V
12/15/04	11:04:44	INFO	GTCC 4 - Analog A	Ref: 1.357 V	Actual: 1.312 V
12/15/04	11:04:44	INFO	GTCC 4 - Analog B	Ref: 2.549 V	Actual: 2.542 V
12/15/04	11:04:44	INFO	GTCC 4 - Digital	Ref: 2.502 V	Actual: 2.477 V
12/15/04	11:04:44	INFO	GTCC 4 - High Voltage	Ref: 137.9 V	Actual: 136.9 V
12/15/04	11:04:44	INFO	GTCC 4 - High Voltage by 2		Actual: 51.79 V
12/15/04	11:04:44	INFO	GTCC 5 - Analog A	Ref: 1.357 V	Actual: 1.323 V
12/15/04	11:04:44	INFO	GTCC 5 - Analog B	Ref: 2.549 V	Actual: 2.551 V
12/15/04	11:04:44	INFO	GTCC 5 - Digital	Ref: 2.502 V	Actual: 2.481 V
12/15/04	11:04:44	INFO	GTCC 5 - High Voltage	Ref: 137.9 V	Actual: 136.7 V
12/15/04	11:04:44	INFO	GTCC 5 - High Voltage by 2		Actual: 49.26 V
12/15/04	11:04:44	INFO	GTCC 6 - Analog A	Ref: 1.357 V	Actual: 1.323 V
12/15/04	11:04:44	INFO	GTCC 6 - Analog B	Ref: 2.549 V	Actual: 2.554 V
12/15/04	11:04:44	INFO	GTCC 6 - Digital	Ref: 2.502 V	Actual: 2.477 V
12/15/04	11:04:44	INFO	GTCC 6 - High Voltage	Ref: 137.9 V	Actual: 139.3 V
12/15/04	11:04:44	INFO	GTCC 6 - High Voltage by 2		Actual: 49.02 V
12/15/04	11:04:44	INFO	GTCC 7 - Analog A	Ref: 1.357 V	Actual: 1.318 V
12/15/04	11:04:44	INFO	GTCC 7 - Analog B	Ref: 2.549 V	Actual: 2.551 V
12/15/04	11:04:44	INFO	GTCC 7 - Digital	Ref: 2.502 V	Actual: 2.478 V
12/15/04	11:04:44	INFO	GTCC 7 - High Voltage	Ref: 137.9 V	Actual: 136.1 V
12/15/04	11:04:44	INFO	GTCC 7 - High Voltage by 2		Actual: 49.69 V
12/15/04	11:04:50	INFO	GCCC 0 - Analog	Ref: 3.330 V	Actual: 3.194 V
12/15/04	11:04:50	INFO	GCCC 0 - Digital	Ref: 3.274 V	Actual: 3.091 V
12/15/04	11:04:50	INFO	GCCC 0 - High Voltage	Ref: 95.69 V	Actual: 98.16 V
12/15/04	11:04:50	INFO	GCCC 1 - Analog	Ref: 3.330 V	Actual: 3.213 V
12/15/04	11:04:50	INFO	GCCC 1 - Digital	Ref: 3.274 V	Actual: 3.145 V
12/15/04	11:04:50	INFO	GCCC 1 - High Voltage	Ref: 95.69 V	Actual: 97.17 V
12/15/04	11:04:50	INFO	GCCC 2 - Analog	Ref: 3.330 V	Actual: 3.194 V
12/15/04	11:04:50	INFO	GCCC 2 - Digital	Ref: 3.274 V	Actual: 3.137 V
12/15/04	11:04:50	INFO	GCCC 2 - High Voltage	Ref: 95.69 V	Actual: 95.94 V
12/15/04	11:04:50	INFO	GCCC 3 - Analog	Ref: 3.330 V	Actual: 3.189 V

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12/15/04 11:04:50 INFO GCCC 3 - Digital Ref: 3.274 V Actual: 3.174 V  
12/15/04 11:04:50 INFO GCCC 3 - High Voltage Ref: 95.69 V Actual: 95.45 V  
12/15/04 11:04:51 INFO All tests successfully completed

temFifo\_20041215\_110510  
12/15/04 11:06:26 INFO All tests successfully completed



func\_20041215\_111041

11:10:46 default tem status 0xb0000  
11:10:46 running temConfigTest  
11:10:46 redundant GEM test missing in temConfigTest  
11:10:46 entering temConfigParity test  
11:10:46 entering tkr tack parity bit test  
11:10:48 entering tkr internal parity bit test  
11:10:50 entering tkr token parity bit test  
11:10:52 entering temCalInternalParityTest  
11:10:52 entering temResponseParity test  
11:10:52 entering temConfigTrigBufTest test  
11:10:54 temConfigCableConTimeoutTest does not exist yet  
11:10:54 done with subtest(s), found 0 errors; total errors: 0  
11:10:56 functional test(s) interrupted, found 0 total errors  
11:10:59 default tem status 0xb0000  
11:10:59 running temConfigTest  
11:10:59 redundant GEM test missing in temConfigTest  
11:10:59 entering temConfigParity test  
11:10:59 entering tkr tack parity bit test  
11:11:01 entering tkr internal parity bit test  
11:11:03 entering tkr token parity bit test  
11:11:05 entering temCalInternalParityTest  
11:11:05 entering temResponseParity test  
11:11:05 entering temConfigTrigBufTest test  
11:11:07 temConfigCableConTimeoutTest does not exist yet  
11:11:07 done with subtest(s), found 0 errors; total errors: 0  
11:11:09 running temDatamasksTest  
11:11:10 entering temDatamasksDiag test  
11:11:11 entering temDatamasksCal test  
11:11:12 entering temDatamasksTkr test  
11:11:13 done with subtest(s), found 0 errors; total errors: 0  
11:11:15 running temStatusTest  
11:11:15 entering temConstatComParity test  
11:11:15 entering temConstatPrimaryParity test  
11:11:15 entering temConstatComPrefixParity test  
11:11:15 entering temConstatTrigMessParity test  
11:11:15 entering temConstatTag test  
11:11:23 entering temConstatCable test  
11:11:30 entering temConstatTimeout test  
11:11:31 entering temConstatComParity test  
11:11:31 entering temConstatRedundantParity test  
11:11:31 entering temConstatRedundantSelected test  
11:11:31 entering temConstatEventsSent test  
11:11:34 done with subtest(s), found 0 errors; total errors: 0  
11:11:36 running temComrespStatTest  
11:11:36 entering temComrespStatTest test  
11:11:36 takes a few minutes as stands  
11:12:11 done with subtest(s), found 0 errors; total errors: 0  
11:12:13 running temCaltrgseqTest  
11:12:13 entering cal TrigSeq test  
11:12:14 done with subtest(s), found 0 errors; total errors: 0  
11:12:16 running temTkrtrgseqTest  
11:12:16 entering gtccTrgSeqTack test  
11:12:17 done with subtest(s), found 0 errors; total errors: 0  
11:12:19 running temAddressTest  
11:12:19 entering temAddress test  
11:12:19 done with subtest(s), found 0 errors; total errors: 0  
11:12:21 running gticPowerSupplyControlTest  
11:12:21 entering gticPowerSupplyControl test  
11:12:32 done with subtest(s), found 0 errors; total errors: 0  
11:12:34 running gticConstatComParityTest  
11:12:34 entering gticConstatComParity test  
11:12:34 done with subtest(s), found 0 errors; total errors: 0  
11:12:36 running gticInputmaskTest

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11:12:36 gticInputmask test does not exist  
11:12:36 done with subtest(s), found 0 errors; total errors: 0  
11:12:38 running gccConfigTest  
11:12:38 entering ccConfigFifoFullCond test  
11:12:38 entering Cal sum subtest  
11:12:40 entering Cal err subtest  
11:12:42 entering Cal data subtest  
11:12:44 entering Cal diag subtest  
11:12:46 done with subtest(s), found 0 errors; total errors: 0  
11:12:48 running gccLayermaskTest  
11:12:48 entering gccLayermaskTest  
11:13:05 done with subtest(s), found 0 errors; total errors: 0  
11:13:07 running gccConfigTest  
11:13:07 entering ccConfigFifoFullCond test  
11:13:07 entering Cal sum subtest  
11:13:09 entering Cal err subtest  
11:13:10 entering Cal data subtest  
11:13:13 entering Cal diag subtest  
11:13:14 done with subtest(s), found 0 errors; total errors: 0  
11:13:16 running gccLatstatFifoTest  
11:13:16 entering gccLatstatFifo test  
11:14:43 done with subtest(s), found 0 errors; total errors: 0  
11:14:45 running gccTimeoutTest  
11:14:45 entering gccTimeout test  
11:14:48 done with subtest(s), found 0 errors; total errors: 0  
11:14:50 running gccTrgalignTest  
11:14:50 gccTrgalign test does not exist: probably a scope test  
11:14:50 done with subtest(s), found 0 errors; total errors: 0  
11:14:52 running gccConfigTest  
11:14:52 entering ccConfigFifoFullCond test  
11:14:52 entering Cal sum subtest  
11:14:53 entering Cal err subtest  
11:14:55 entering Cal data subtest  
11:14:57 entering Cal diag subtest  
11:14:59 done with subtest(s), found 0 errors; total errors: 0  
11:15:01 running gtccInputmaskTest  
11:15:01 entering gtccInputmaskTest  
11:15:10 done with subtest(s), found 0 errors; total errors: 0  
11:15:12 running gtccConfigTest  
11:15:12 entering gtccConfigCableLength test  
11:15:13 entering ccConfigFifoFullCond test  
11:15:13 entering tkr sum subtest  
11:15:15 entering tkr diag subtest  
11:15:43 entering tkr tot subtest  
11:15:46 entering tkr err subtest  
11:15:49 entering tkr data subtest  
11:15:50 done with subtest(s), found 0 errors; total errors: 0  
11:15:52 running gtccLatstatFifoTest  
11:15:52 entering gtccLatstatFifo test  
11:16:01 n.b.: in gtccLatstatFifo; it is not possible to test data fifo write full bits  
11:17:05 done with subtest(s), found 0 errors; total errors: 0  
11:17:07 running gtccTimeoutTest  
11:17:07 entering gtccTimeout test  
11:17:28 done with subtest(s), found 0 errors; total errors: 0  
11:17:30 running gtccTrgalignTest  
11:17:30 gtccTrgalign test does not exist: probably a scope test  
11:17:30 done with subtest(s), found 0 errors; total errors: 0  
11:17:32 done with functional test(s), found 0 total errors

tps\_0386\_612\_20041215\_105942

10:59:43 TPS calibration data for TPS 0386  
10:59:44 please wait approx. 30 sec for the system to settle  
11:00:09 dv 0.003860: current 0.130000  
11:00:13 dv 0.009021: current 0.470000  
11:00:19 dv 0.012064: current 0.672000  
11:00:23 dv 0.017225: current 1.007000  
11:00:23 slope,intercept

11:00:23 65.658863,-0.122454