COVER SHEET

Program: GLAST

Procedure Number: LAT-TD-04085

Procedure Title: TEM/TPS Performance Test Procedure

Paragraph Number: _____

Paragraph Title: _____

Unit S/N: GLAT1754

TEST READINESS REVIEW COMPLETED AND APPROVED BY THE FOLLOWING:

Test Director: _____ Date: _____

Quality Assurance: _____ LAT 10 QA Date: 1.12.05

Test Conductor: _____ Date: 1/12/05

REVIEWED AND APPROVED BY THE FOLLOWING:

Test Director: _____ Date: _____

Quality Assurance: _____ LAT 10 QA Date: 1.12.05

Test Conductor: _____ Date: 1/12/05

TEST DATA SHEET	Unit S/N: GLAT1754	Date/Temperature: 1/11/05 RT
Title: 5.1.3 Test Equipment	Operator: JL	QA: LAT 10 04

Para./ Step	Test Equipment Description, Manufacturer	Model/LAT Number	Serial/Rev. Number	*Cal./Val. Date
5.1.3.1 - 1	**Record Model/LAT number, Serial/Revision number, Calibration due dates and Validation date for all equipment used in this procedure:**			
	VME Crate, Dawn VME Products	11-1011777-2119 VME64x (series 767)	GLAT1132	12.8.05
	VME, TST-STP Trans card	LAT-DS-00999	GLAT0216	
	VME SBC MVME2304 card, Motorola	PN MVME2304-0123	GLAT0305	
	VME LCB Mezzanine card	LAT-TD-00860	GLAT0872	
	Software for the local PC	LATTE P04-04-01 www-glast.slac.stanford.edu/IntegrationTest/ONLINE/updates/	P04-04-01	
	Software for the local PC	TEMPROD V00-00-00	OK	12.8.05
	DC Power supply #1, BK Precision	BK 1697	GLAT1485	8/05
	DC Power supply #2, BK Precision	BK 1697	GLAT1336	8/05
	28 Volt supply cable	LAT-DS-03246	N/A	12.8.05
	PS Control cable	LAT-DS-04831	GLAT1420	9/05
	TEM to GASU cable	LAT-DS-02106	GLAT1421	9/05
	LCB Transition board cable	LAT-DS-03247	GLAT1314	12.8.05
	TEM Test Board Assembly	LAT-DS-04465	GLAT0477	
	TEM Test board cooling fan assembly	LAT-DS-03567	GLAT0022	
	CAT5 Ethernet cable	TRD855PL-50	NA	
	RS-232 Cable	TDC003-7 (RECO98M connectors)	NA	
	Ground jumper, Banana, Pomona	B-12-0	NA	12.8.05
	PS extension cable	LAT-DS-04629	GLAT1397	9/05
	Digital Multimeter, Fluke/Meterman	87-III/38XR SLAC00004	GLAT1666	11/05
	Connector Savers (28 pin), L Com	DGBH28MF	NA	12.8.05

TEST DATA SHEET	Unit S/N: GLAT1754	Date/Temperature: 1/11/05 RT
Title: 5.1.3 Test Equipment	Operator: JL	QA: LAT 10 QA

Para./ Step	Test Equipment Description, Manufacturer	Model/LAT Number	Serial/Rev. Number	*Cal./Val. Date
5.1.3.1 - 1	**Record Model/LAT number, Serial/Revision number, Calibration due dates and Validation date for all equipment used in this procedure:**			
	Connector Savers (51 pin), Glenair	MWDM2L-51USP1	NA	12.8.05
	Connector Savers (69 pin), SLAC	LAT-DS-04724	NA	12.8.05
	Connector Savers (78 pin), L Com	DGBH78MF	NA	12.8.05
	Breakout Box Assembly (BOB) (78 pin), SLAC	LAT-DS-03580	GLAT1388	9/05
	Breakout Cable (BOC), SLAC	LAT-DS-04273	GLAT1431	9/05
	Breakout Cable (BOC), SLAC	LAT-DS-04275	GLAT1441	9/05
	Load	LAT-DS-04822	GLAT1475	10/05
	Load	LAT-DS-04823	GLAT1476	10/05
	1 MHz Filter	LAT-DS-04767	GLAT1504	12.8.05
	Noise Measurement Adapter, 51-Pin, SLAC	LAT-DS-04821	GLAT1479	10/05
	Noise Measurement Adapter, 69-Pin, SLAC	LAT-DS-04820	GLAT1478	10/05
	True RMS Volt Meter, Agilent (HP)	3400A	GLAT1228	7.05
	Delay Line, Lemo To Bnc 4N, from SLAC Stores	STORES ID #078697	NA	12.8.05

* This column is used to enter the date that equipment is validated, when validated equipment is recorded in this data sheet.

TEST DATA SHEET	Unit S/N: CLAT1754	Date/Temperature: 1/11/05 RT
Title: 5.1.4 Participant List	Operator: JL	QA: LAT 10 QA

Para./ Step	Title	Print Name	Signature
5.1.4 - 1	**Record names of all personnel that take part in the test/operation:**		
	Engineer	Jeffrey Ludvik	
	QE	PAT LUJAN	

TEST DATA SHEET	Unit S/N: GLAT1754	Date: 1/11/05 RT
Title: 5.2 Pre-Operation Verifications	Operator: JL	QA: LAT 10 QA

Step	Description	Requirement	Units	Data
5.2	Pre-Operation Verifications			
-1	Notify QAE.	OK	OK/NG	OK
-2	Test Readiness Review is done.	OK	OK/NG	OK
-3	Record the UUT equipment:			
	TEM Part number	NA	NA	LAT-DS-01481
	TEM Serial number	NA	NA	GLAT1748
	TEM LAT Bay location	NA	NA	NA
	TPS Part number	NA	NA	LAT-DS-01482
	TPS Serial number	NA	NA	GLAT1751
	TPS LAT Bay location	NA	NA	NA
-4	Ensure that the LAT or EGSE power is off.	OFF	ON/OFF	OFF
-5	All connector savers are installed on the flight connections.	OK	OK/NG	OK
-6	The test equipment and participant lists have been completed.	OK	OK/NG	OK

TEST DATA SHEET	Unit S/N: GLAT1754	Date/Temperature: 1/11/05 RT
Paragraph: 5.4 Calibration Tests	Operator: JL	QA: LAT 10 QA

Step	Description	Requirement	Units	Data
5.4.1	Test: CAL Calibration High Voltage Test Procedure			
-1	Verify that the power is off to power supply #1 and the VME Crate.	OK	OK/NG	OK
-3	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-4	Measure DMM lead resistance.	<2.0	Ω	0.2
-5	Measure BOB to ground.	<2.0	Ω	0.5
-6	Remove all shorting plugs from BOBs.	OK	OK/NG	OK
-7	Measure UUT to ground.	<2.0	Ω	0.9
-8	Measure equipment to ground.	<2.0	Ω	0.6
-9	Connect BOB and configure DMM.	OK	OK/NG	OK
-31	Verify the test passed by green indicator and no errors in the Messages box.	OK	OK/NG	OK
-32	Attach printout of the test log file to this data package.	OK	OK/NG	OK

TEST DATA SHEET	Unit S/N: GLAT1754	Date/Temperature: 1/11/05 RT
Paragraph: 5.4 Calibration Tests	Operator: JL	QA: LAT 10 QA

Step	Description	Requirement	Units	Data
5.4.2	Test: TRK Calibration High Voltage Test Procedure			
-1	Verify that the power is off to power supply #1 and the VME Crate.	OK	OK/NG	OK
-3	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-4	Measure DMM lead resistance.	< 2.0	Ω	0.2
-5	Measure BOB to ground.	< 2.0	Ω	0.3
-6	Remove all shorting plugs from BOBs.	OK	OK/NG	OK
-7	Measure UUT to ground.	< 2.0	Ω	0.7
-8	Measure equipment to ground.	< 2.0	Ω	0.7
-9	Connect BOB and configure DMM.	OK	OK/NG	OK
-31	Verify the test passed by green indicator and no errors in the Messages box.	OK	OK/NG	OK
-32	Attach printout of the test log file to this data package.	OK	OK/NG	OK
-				
-				
-				
-				

TEST DATA SHEET	Unit S/N: GLAT1754	Date/Temperature: 1/11/05 RT
Paragraph: 5.4 Calibration Tests	Operator: JL	QA: LAT 10 QA

Step	Description	Requirement	Units	Data
5.4.3	Test: TPS Calibration Tower Current Test Procedure			
-1	Verify that the power is off to power supply #1 and the VME Crate.	OK	OK/NG	OK
-2	Disconnect the Test Board Cooling Fan.	OK	OK/NG	OK
-4	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-5	Measure DMM lead resistance.	< 2.0	Ω	0.6
-6	Measure UUT to ground.	< 2.0	Ω	0.8
-7	Measure equipment to ground.	< 2.0	Ω	0.7
-28	Verify the test passed by green indicator and no errors in the Messages box.	OK	OK/NG	OK
-29	Attach printout of the test log file to this data package.	OK	OK/NG	OK

TEST DATA SHEET	Unit S/N: CLAT1754	Date: 1/12/05
Title: 5.5 Main Tests	Operator: JL	QA: LAT TO QA

Step	Description	Requirement	Units	Data
5.5.1	Main Tests Setup Procedure			
-1	Verify that the power is off to power supply #1 and the VME Crate.	OK	OK/NG	OK
-3	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-4	Measure DMM lead resistance.	< 2.0	Ω	0.2
-5	Measure UUT to ground.	< 2.0	Ω	0.8
-6	Measure equipment to ground.	< 2.0	Ω	0.8
-12	Record the current draw at the external power supply #1.	0.100 - 0.130	Amps	0.129

TEST DATA SHEET	Unit S/N: GLAST1754	Date/Temperature: 1/17/05 RT
Paragraph: 5.5 Main Tests	Operator: JL	QA: LAT TO QA

Step	Description	Requirement	Units	Data
5.5.2	Monitor Margin and Bias Test Procedure			
-11	Verify the test passed by green indicator and no errors in the Messages box on the Margin and Bias Test window.	OK	OK/NG	OK
-12	Attach printout of the Monitor Margin and Bias Test log file to this data package.	OK	OK/NG	OK
5.5.3	Temperature Monitor Test			
-11	Verify the test passed by green indicator and no errors in the Messages box on the Temperature Tests window.	OK	OK/NG	OK
-12	Attach printout of the Temperature Monitor Test log file to this data package.	OK	OK/NG	OK
5.5.4	Basic Test			
-8	Verify all tests passed by green indicators and "0" for Communication Errors and Event Errors on the Main Panel tab.	OK	OK/NG	OK
-9	Attach printout of the Basic Test log file to this data package.	OK	OK/NG	OK
5.5.5	Front End Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the Main Panel tab.	OK	OK/NG	OK
-9	Attach printout of the Front End Test log file to this data package.	OK	OK/NG	OK
5.5.6	FIFO Test			
-8	Verify all tests passed by green indicators and "0" for Total Errors on the FIFO Test window.	OK	OK/NG	OK
-9	Attach printout of the FIFO Test log file to this data package.	OK	OK/NG	OK

see page 94

TEST DATA SHEET		Unit S/N: GLAT1754		Date/Temperature: 1/11/05 RT
Paragraph: 5.6 Functional Test Procedure		Operator: JL		QA: LAT TO QA
Step	Description	Requirement	Units	Data
5.6	Functional Test			
-8	Verify all tests passed by green indicators and no errors in the Messages box on the Functional Test window.	OK	OK/NG	OK
-9	Attach printout of the Functional Test log file to this data package.	OK	OK/NG	OK

TEST DATA SHEET	Unit S/N: GLAT1754	Date: 1/12/05
Title: 5.7 Noise Tests	Operator: JL	QA: LAT IO QA

Step	Description	Requirement	Units	Data
5.7.2	CAL Noise Test Procedure			
-1	Verify that the power is off to power supply #1 and 2 and the VME Crate.	OK	OK/NG	OK
-3	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-4	Measure DMM lead resistance.	< 2.0	Ω	0.2
-5	Measure UUT to ground.	< 2.0	Ω	0.8
-6	Measure equipment to ground.	< 2.0	Ω	0.8
-7	Connect J4 of the adaptor.	OK	OK/NG	OK
-8	RMS meter has been running 20 minutes.	OK	OK/NG	OK
-9	Set the RMS meter to the 1 mV range.	OK	OK/NG	OK
-30	Record the CAL bias (HV) noise.	<500µ	Volts	<100 mV
-31	Turn off the CAL bias.	OK	OK/NG	OK
-33	Connect J2 of the adaptor.	OK	OK/NG	OK
-34	Record the CAL 3.3 analog voltage noise.	<150µ	Volts	<100 mV
-36	Connect J3 of the adaptor.	OK	OK/NG	OK
-37	Record the CAL 3.3 digital voltage noise.	<200µ	Volts	<100 mV
-39	Verify all tests passed by green indicators and no errors in the Messages box on the Functional Test window.	OK	OK/NG	OK
-40	Attach printout of the test log file to this data package.	OK	OK/NG	OK

TEST DATA SHEET	Unit S/N: GLAT1754	Date: 1/12/05
Title: 5.7 Noise Tests	Operator: JL	QA: LAT TO QA

Step	Description	Requirement	Units	Data
5.7.3	TKR Noise Test Procedure			
-1	Verify that the power is off to power supply #1 and 2 and the VME Crate.	OK	OK/NG	OK
-3	Set DMM to autoranging for resistance.	OK	OK/NG	OK
-4	Measure DMM lead resistance.	< 2.0	Ω	0.2
-5	Measure UUT to ground.	< 2.0	Ω	0.8
-6	Measure equipment to ground.	< 2.0	Ω	0.8
-7	Connect J5 of the adaptor.	OK	OK/NG	OK
-8	Ensure that the RMS meter has been running 20 minutes.	OK	OK/NG	OK
-9	Set the RMS meter to the 1 mV range.	OK	OK/NG	OK
-31	Record the TKR Bias (HV) noise.	<500μ	Volts	<100 mV
-32	Turn off the TKR bias.	OK	OK/NG	OK
-34	Connect J2 of the adaptor.	OK	OK/NG	OK
-35	Record the TKR 2.5 analog voltage noise.	<150μ	Volts	<100mV
-37	Connect J3 of the adaptor to the RMS meter.	OK	OK/NG	OK
-38	Record the TKR 1.5 analog voltage noise.	<150μ	Volts	<100mV
-40	Connect J4 of the adaptor.	OK	OK/NG	OK
-41	Record the TKR 2.5 digital voltage noise.	<150μ	Volts	<100mV
-43	Verify all tests passed by green indicators and no errors in the Messages box on the Functional Test window.	OK	OK/NG	OK
-44	Attach printout of the Functional Test log file to this data package.	OK	OK/NG	OK

1/11/05 Installed J2 (TPS) (connector saver 

Test doc: labeled JC0 - JC3
JT0 - JT7

Silkscreen labeled: JC1 - JC4
JT1 - JT8

from page 90 TKR Analog B: req change to 2.35 - 2.78

CAL Bias current: req change to 0.000400 - 0.001000

temFifo_20050111_173932

01/11/05 17:40:47 INFO All tests successfuly completed

tkr_GLAT1754_GLAT1748_20050111_152935

```
15:29:48  ,bias_voltage,dvm_current,read_current
15:29:48  ,69.7429664225,1.82,1.88596686538
15:30:16  ,140.029655678,3.63,3.7728042328
15:30:29  ,104.944179487,2.72,2.82953063277
15:30:29  ,slope_in_mA(dvm)/mA(tem),intercept_in_mA(dmv)
15:30:29  ,0.959276885418,0.00912278434883
15:30:29  ,,,,,bias_voltage_(V),current_read_by_tem_(mA),dvm_extapolated_current
15:30:33  ,,,,,0.578129426129,5.02485216309,4.82934731704
15:30:37  ,,,,,7.95421245421,3.59037360243,3.45328519118
15:30:41  ,,,,,15.3534798535,2.15207450502,2.07355811271
15:30:44  ,,,,,22.752993895,0.725370011252,0.704953469519
15:30:48  ,,,,,26.6989615385,0.7133885178,0.693459899797
15:30:52  ,,,,,33.2151263736,0.894755201226,0.867440766992
15:30:56  ,,,,,39.7138412698,1.07225298666,1.03771028978
15:31:00  ,,,,,46.2487509158,1.24690955014,1.20525429401
15:31:03  ,,,,,52.7963009768,1.42375445905,1.37489752743
15:31:07  ,,,,,59.3641990232,1.59883418325,1.54284745995
15:31:11  ,,,,,65.9150787546,1.77729919318,1.71404481884
15:31:15  ,,,,,72.4644786325,1.95636871843,1.88582207529
15:31:18  ,,,,,79.0488400488,2.13678026766,2.05888670434
15:31:22  ,,,,,85.6406007326,2.31039706481,2.22543328476
15:31:26  ,,,,,92.2163913309,2.49529411765,2.40280075373
15:31:30  ,,,,,98.8071654457,2.67171586583,2.57203805885
15:31:34  ,,,,,105.382832723,2.85273193038,2.74568258546
15:31:37  ,,,,,111.978847985,3.03361500156,2.9191995346
15:31:41  ,,,,,118.578686203,3.21088307118,3.08924869631
15:31:45  ,,,,,125.184443834,3.38359309536,3.25492543039
15:31:49  ,,,,,131.778547619,3.56445198592,3.42841918363
15:31:53  ,,,,,138.364327228,3.7359892504,3.59297091643
```

temFe_20050111_173802

```
01/11/05 17:38:11 INFO  GTCC 0 - Analog A          Ref: 1.585 V    Actual: 1.500 V
01/11/05 17:38:11 INFO  GTCC 0 - Analog B          Ref: 2.752 V    Actual: 2.730 V
01/11/05 17:38:11 INFO  GTCC 0 - Digital           Ref: 2.694 V    Actual: 2.604 V
01/11/05 17:38:11 INFO  GTCC 0 - High Voltage      Ref: 125.8 V    Actual: 124.5 V
01/11/05 17:38:11 INFO  GTCC 0 - High Voltage by 2                 Actual: 48.77 V

01/11/05 17:38:11 INFO  GTCC 1 - Analog A          Ref: 1.585 V    Actual: 1.509 V
01/11/05 17:38:11 INFO  GTCC 1 - Analog B          Ref: 2.752 V    Actual: 2.737 V
01/11/05 17:38:11 INFO  GTCC 1 - Digital           Ref: 2.694 V    Actual: 2.622 V
01/11/05 17:38:11 INFO  GTCC 1 - High Voltage      Ref: 125.8 V    Actual: 124.8 V
01/11/05 17:38:11 INFO  GTCC 1 - High Voltage by 2                 Actual: 45.69 V

01/11/05 17:38:11 INFO  GTCC 2 - Analog A          Ref: 1.585 V    Actual: 1.511 V
01/11/05 17:38:11 INFO  GTCC 2 - Analog B          Ref: 2.752 V    Actual: 2.742 V
01/11/05 17:38:11 INFO  GTCC 2 - Digital           Ref: 2.694 V    Actual: 2.627 V
01/11/05 17:38:11 INFO  GTCC 2 - High Voltage      Ref: 125.8 V    Actual: 124.4 V
01/11/05 17:38:11 INFO  GTCC 2 - High Voltage by 2                 Actual: 44.88 V

01/11/05 17:38:11 INFO  GTCC 3 - Analog A          Ref: 1.585 V    Actual: 1.529 V
01/11/05 17:38:11 INFO  GTCC 3 - Analog B          Ref: 2.752 V    Actual: 2.746 V
01/11/05 17:38:11 INFO  GTCC 3 - Digital           Ref: 2.694 V    Actual: 2.644 V
01/11/05 17:38:11 INFO  GTCC 3 - High Voltage      Ref: 125.8 V    Actual: 124.8 V
01/11/05 17:38:11 INFO  GTCC 3 - High Voltage by 2                 Actual: 46.18 V

01/11/05 17:38:11 INFO  GTCC 4 - Analog A          Ref: 1.585 V    Actual: 1.544 V
01/11/05 17:38:11 INFO  GTCC 4 - Analog B          Ref: 2.752 V    Actual: 2.754 V
01/11/05 17:38:11 INFO  GTCC 4 - Digital           Ref: 2.694 V    Actual: 2.671 V
01/11/05 17:38:11 INFO  GTCC 4 - High Voltage      Ref: 125.8 V    Actual: 123.7 V
01/11/05 17:38:11 INFO  GTCC 4 - High Voltage by 2                 Actual: 45.13 V

01/11/05 17:38:11 INFO  GTCC 5 - Analog A          Ref: 1.585 V    Actual: 1.553 V
01/11/05 17:38:11 INFO  GTCC 5 - Analog B          Ref: 2.752 V    Actual: 2.757 V
01/11/05 17:38:11 INFO  GTCC 5 - Digital           Ref: 2.694 V    Actual: 2.669 V
01/11/05 17:38:11 INFO  GTCC 5 - High Voltage      Ref: 125.8 V    Actual: 126.7 V
01/11/05 17:38:11 INFO  GTCC 5 - High Voltage by 2                 Actual: 44.64 V

01/11/05 17:38:11 INFO  GTCC 6 - Analog A          Ref: 1.585 V    Actual: 1.545 V
01/11/05 17:38:11 INFO  GTCC 6 - Analog B          Ref: 2.752 V    Actual: 2.752 V
01/11/05 17:38:11 INFO  GTCC 6 - Digital           Ref: 2.694 V    Actual: 2.667 V
01/11/05 17:38:11 INFO  GTCC 6 - High Voltage      Ref: 125.8 V    Actual: 124.3 V
01/11/05 17:38:11 INFO  GTCC 6 - High Voltage by 2                 Actual: 44.76 V

01/11/05 17:38:11 INFO  GTCC 7 - Analog A          Ref: 1.585 V    Actual: 1.534 V
01/11/05 17:38:11 INFO  GTCC 7 - Analog B          Ref: 2.752 V    Actual: 2.741 V
01/11/05 17:38:11 INFO  GTCC 7 - Digital           Ref: 2.694 V    Actual: 2.661 V
01/11/05 17:38:11 INFO  GTCC 7 - High Voltage      Ref: 125.8 V    Actual: 124.4 V
01/11/05 17:38:11 INFO  GTCC 7 - High Voltage by 2                 Actual: 47.04 V

01/11/05 17:38:17 INFO  GCCC 0 - Analog            Ref: 3.382 V    Actual: 3.252 V
01/11/05 17:38:17 INFO  GCCC 0 - Digital           Ref: 3.284 V    Actual: 3.145 V
01/11/05 17:38:17 INFO  GCCC 0 - High Voltage      Ref: 32.68 V    Actual: 33.29 V

01/11/05 17:38:17 INFO  GCCC 1 - Analog            Ref: 3.382 V    Actual: 3.262 V
01/11/05 17:38:17 INFO  GCCC 1 - Digital           Ref: 3.284 V    Actual: 3.128 V
01/11/05 17:38:17 INFO  GCCC 1 - High Voltage      Ref: 32.68 V    Actual: 33.97 V

01/11/05 17:38:17 INFO  GCCC 2 - Analog            Ref: 3.382 V    Actual: 3.242 V
01/11/05 17:38:17 INFO  GCCC 2 - Digital           Ref: 3.284 V    Actual: 3.242 V
01/11/05 17:38:17 INFO  GCCC 2 - High Voltage      Ref: 32.68 V    Actual: 33.35 V

01/11/05 17:38:17 INFO  GCCC 3 - Analog            Ref: 3.382 V    Actual: 3.262 V
01/11/05 17:38:17 INFO  GCCC 3 - Digital           Ref: 3.284 V    Actual: 3.199 V
01/11/05 17:38:17 INFO  GCCC 3 - High Voltage      Ref: 32.68 V    Actual: 33.78 V
```

```
01/11/05 17:38:26 INFO  GTCC 0 - Analog A          Ref: 1.584 V    Actual: 1.499 V
01/11/05 17:38:26 INFO  GTCC 0 - Analog B          Ref: 2.75 V    Actual: 2.730 V
01/11/05 17:38:26 INFO  GTCC 0 - Digital           Ref: 2.690 V    Actual: 2.603 V
01/11/05 17:38:26 INFO  GTCC 0 - High Voltage      Ref: 124.5 V    Actual: 123.4 V
01/11/05 17:38:26 INFO  GTCC 0 - High Voltage by 2                 Actual: 48.34 V

01/11/05 17:38:26 INFO  GTCC 1 - Analog A          Ref: 1.584 V    Actual: 1.509 V
01/11/05 17:38:26 INFO  GTCC 1 - Analog B          Ref: 2.75 V    Actual: 2.736 V
01/11/05 17:38:26 INFO  GTCC 1 - Digital           Ref: 2.690 V    Actual: 2.620 V
01/11/05 17:38:26 INFO  GTCC 1 - High Voltage      Ref: 124.5 V    Actual: 123.6 V
01/11/05 17:38:26 INFO  GTCC 1 - High Voltage by 2                 Actual: 45.32 V

01/11/05 17:38:26 INFO  GTCC 2 - Analog A          Ref: 1.584 V    Actual: 1.510 V
01/11/05 17:38:26 INFO  GTCC 2 - Analog B          Ref: 2.75 V    Actual: 2.742 V
01/11/05 17:38:26 INFO  GTCC 2 - Digital           Ref: 2.690 V    Actual: 2.627 V
01/11/05 17:38:26 INFO  GTCC 2 - High Voltage      Ref: 124.5 V    Actual: 123.3 V
01/11/05 17:38:26 INFO  GTCC 2 - High Voltage by 2                 Actual: 44.51 V

01/11/05 17:38:26 INFO  GTCC 3 - Analog A          Ref: 1.584 V    Actual: 1.528 V
01/11/05 17:38:26 INFO  GTCC 3 - Analog B          Ref: 2.75 V    Actual: 2.744 V
01/11/05 17:38:26 INFO  GTCC 3 - Digital           Ref: 2.690 V    Actual: 2.643 V
01/11/05 17:38:26 INFO  GTCC 3 - High Voltage      Ref: 124.5 V    Actual: 123.6 V
01/11/05 17:38:26 INFO  GTCC 3 - High Voltage by 2                 Actual: 45.81 V

01/11/05 17:38:26 INFO  GTCC 4 - Analog A          Ref: 1.584 V    Actual: 1.543 V
01/11/05 17:38:26 INFO  GTCC 4 - Analog B          Ref: 2.75 V    Actual: 2.752 V
01/11/05 17:38:26 INFO  GTCC 4 - Digital           Ref: 2.690 V    Actual: 2.671 V
01/11/05 17:38:26 INFO  GTCC 4 - High Voltage      Ref: 124.5 V    Actual: 122.5 V
01/11/05 17:38:26 INFO  GTCC 4 - High Voltage by 2                 Actual: 44.70 V

01/11/05 17:38:26 INFO  GTCC 5 - Analog A          Ref: 1.584 V    Actual: 1.550 V
01/11/05 17:38:26 INFO  GTCC 5 - Analog B          Ref: 2.75 V    Actual: 2.755 V
01/11/05 17:38:26 INFO  GTCC 5 - Digital           Ref: 2.690 V    Actual: 2.667 V
01/11/05 17:38:26 INFO  GTCC 5 - High Voltage      Ref: 124.5 V    Actual: 125.5 V
01/11/05 17:38:26 INFO  GTCC 5 - High Voltage by 2                 Actual: 44.27 V

01/11/05 17:38:26 INFO  GTCC 6 - Analog A          Ref: 1.584 V    Actual: 1.544 V
01/11/05 17:38:26 INFO  GTCC 6 - Analog B          Ref: 2.75 V    Actual: 2.752 V
01/11/05 17:38:26 INFO  GTCC 6 - Digital           Ref: 2.690 V    Actual: 2.667 V
01/11/05 17:38:26 INFO  GTCC 6 - High Voltage      Ref: 124.5 V    Actual: 123.1 V
01/11/05 17:38:26 INFO  GTCC 6 - High Voltage by 2                 Actual: 44.39 V

01/11/05 17:38:26 INFO  GTCC 7 - Analog A          Ref: 1.584 V    Actual: 1.533 V
01/11/05 17:38:26 INFO  GTCC 7 - Analog B          Ref: 2.75 V    Actual: 2.739 V
01/11/05 17:38:26 INFO  GTCC 7 - Digital           Ref: 2.690 V    Actual: 2.660 V
01/11/05 17:38:26 INFO  GTCC 7 - High Voltage      Ref: 124.5 V    Actual: 123.3 V
01/11/05 17:38:26 INFO  GTCC 7 - High Voltage by 2                 Actual: 46.61 V

01/11/05 17:38:31 INFO  GCCC 0 - Analog            Ref: 3.378 V    Actual: 3.252 V
01/11/05 17:38:31 INFO  GCCC 0 - Digital           Ref: 3.350 V    Actual: 3.091 V
01/11/05 17:38:31 INFO  GCCC 0 - High Voltage      Ref: 89.65 V    Actual: 90.82 V

01/11/05 17:38:32 INFO  GCCC 1 - Analog            Ref: 3.378 V    Actual: 3.262 V
01/11/05 17:38:32 INFO  GCCC 1 - Digital           Ref: 3.350 V    Actual: 3.213 V
01/11/05 17:38:32 INFO  GCCC 1 - High Voltage      Ref: 89.65 V    Actual: 91.75 V

01/11/05 17:38:32 INFO  GCCC 2 - Analog            Ref: 3.378 V    Actual: 3.242 V
01/11/05 17:38:32 INFO  GCCC 2 - Digital           Ref: 3.350 V    Actual: 3.218 V
01/11/05 17:38:32 INFO  GCCC 2 - High Voltage      Ref: 89.65 V    Actual: 89.28 V

01/11/05 17:38:32 INFO  GCCC 3 - Analog            Ref: 3.378 V    Actual: 3.262 V
01/11/05 17:38:32 INFO  GCCC 3 - Digital           Ref: 3.350 V    Actual: 3.157 V
```

```
01/11/05 17:38:32 INFO  GCCC 3 - High Voltage      Ref: 89.65 V    Actual: 89.77 V

01/11/05 17:38:40 INFO  GTCC 0 - Analog A          Ref: 1.584 V    Actual: 1.499 V
01/11/05 17:38:40 INFO  GTCC 0 - Analog B          Ref: 2.75 V     Actual: 2.730 V
01/11/05 17:38:40 INFO  GTCC 0 - Digital           Ref: 2.691 V    Actual: 2.603 V
01/11/05 17:38:40 INFO  GTCC 0 - High Voltage      Ref: 123.8 V    Actual: 122.7 V
01/11/05 17:38:40 INFO  GTCC 0 - High Voltage by 2                 Actual: 48.09 V

01/11/05 17:38:40 INFO  GTCC 1 - Analog A          Ref: 1.584 V    Actual: 1.509 V
01/11/05 17:38:40 INFO  GTCC 1 - Analog B          Ref: 2.75 V     Actual: 2.736 V
01/11/05 17:38:40 INFO  GTCC 1 - Digital           Ref: 2.691 V    Actual: 2.620 V
01/11/05 17:38:40 INFO  GTCC 1 - High Voltage      Ref: 123.8 V    Actual: 122.9 V
01/11/05 17:38:40 INFO  GTCC 1 - High Voltage by 2                 Actual: 45.07 V

01/11/05 17:38:40 INFO  GTCC 2 - Analog A          Ref: 1.584 V    Actual: 1.510 V
01/11/05 17:38:40 INFO  GTCC 2 - Analog B          Ref: 2.75 V     Actual: 2.742 V
01/11/05 17:38:40 INFO  GTCC 2 - Digital           Ref: 2.691 V    Actual: 2.627 V
01/11/05 17:38:40 INFO  GTCC 2 - High Voltage      Ref: 123.8 V    Actual: 122.6 V
01/11/05 17:38:40 INFO  GTCC 2 - High Voltage by 2                 Actual: 44.27 V

01/11/05 17:38:40 INFO  GTCC 3 - Analog A          Ref: 1.584 V    Actual: 1.528 V
01/11/05 17:38:40 INFO  GTCC 3 - Analog B          Ref: 2.75 V     Actual: 2.744 V
01/11/05 17:38:40 INFO  GTCC 3 - Digital           Ref: 2.691 V    Actual: 2.643 V
01/11/05 17:38:40 INFO  GTCC 3 - High Voltage      Ref: 123.8 V    Actual: 122.9 V
01/11/05 17:38:40 INFO  GTCC 3 - High Voltage by 2                 Actual: 45.56 V

01/11/05 17:38:40 INFO  GTCC 4 - Analog A          Ref: 1.584 V    Actual: 1.543 V
01/11/05 17:38:40 INFO  GTCC 4 - Analog B          Ref: 2.75 V     Actual: 2.752 V
01/11/05 17:38:40 INFO  GTCC 4 - Digital           Ref: 2.691 V    Actual: 2.671 V
01/11/05 17:38:40 INFO  GTCC 4 - High Voltage      Ref: 123.8 V    Actual: 121.9 V
01/11/05 17:38:40 INFO  GTCC 4 - High Voltage by 2                 Actual: 44.51 V

01/11/05 17:38:40 INFO  GTCC 5 - Analog A          Ref: 1.584 V    Actual: 1.550 V
01/11/05 17:38:40 INFO  GTCC 5 - Analog B          Ref: 2.75 V     Actual: 2.755 V
01/11/05 17:38:40 INFO  GTCC 5 - Digital           Ref: 2.691 V    Actual: 2.669 V
01/11/05 17:38:40 INFO  GTCC 5 - High Voltage      Ref: 123.8 V    Actual: 124.8 V
01/11/05 17:38:40 INFO  GTCC 5 - High Voltage by 2                 Actual: 44.02 V

01/11/05 17:38:40 INFO  GTCC 6 - Analog A          Ref: 1.584 V    Actual: 1.544 V
01/11/05 17:38:40 INFO  GTCC 6 - Analog B          Ref: 2.75 V     Actual: 2.752 V
01/11/05 17:38:40 INFO  GTCC 6 - Digital           Ref: 2.691 V    Actual: 2.666 V
01/11/05 17:38:40 INFO  GTCC 6 - High Voltage      Ref: 123.8 V    Actual: 122.4 V
01/11/05 17:38:40 INFO  GTCC 6 - High Voltage by 2                 Actual: 44.14 V

01/11/05 17:38:40 INFO  GTCC 7 - Analog A          Ref: 1.584 V    Actual: 1.533 V
01/11/05 17:38:40 INFO  GTCC 7 - Analog B          Ref: 2.75 V     Actual: 2.739 V
01/11/05 17:38:40 INFO  GTCC 7 - Digital           Ref: 2.691 V    Actual: 2.660 V
01/11/05 17:38:40 INFO  GTCC 7 - High Voltage      Ref: 123.8 V    Actual: 122.6 V
01/11/05 17:38:40 INFO  GTCC 7 - High Voltage by 2                 Actual: 46.36 V

01/11/05 17:38:46 INFO  GCCC 0 - Analog            Ref: 3.377 V    Actual: 3.252 V
01/11/05 17:38:46 INFO  GCCC 0 - Digital           Ref: 3.252 V    Actual: 3.169 V
01/11/05 17:38:46 INFO  GCCC 0 - High Voltage      Ref: 89.71 V    Actual: 90.82 V

01/11/05 17:38:46 INFO  GCCC 1 - Analog            Ref: 3.377 V    Actual: 3.262 V
01/11/05 17:38:46 INFO  GCCC 1 - Digital           Ref: 3.252 V    Actual: 3.164 V
01/11/05 17:38:46 INFO  GCCC 1 - High Voltage      Ref: 89.71 V    Actual: 91.75 V

01/11/05 17:38:46 INFO  GCCC 2 - Analog            Ref: 3.377 V    Actual: 3.242 V
01/11/05 17:38:46 INFO  GCCC 2 - Digital           Ref: 3.252 V    Actual: 3.150 V
01/11/05 17:38:46 INFO  GCCC 2 - High Voltage      Ref: 89.71 V    Actual: 89.28 V

01/11/05 17:38:46 INFO  GCCC 3 - Analog            Ref: 3.377 V    Actual: 3.262 V
```

temFe_20050111_173802

```
01/11/05 17:38:46 INFO  GCCC 3 - Digital          Ref: 3.252 V    Actual: 3.233 V
01/11/05 17:38:46 INFO  GCCC 3 - High Voltage     Ref: 89.71 V    Actual: 89.77 V

01/11/05 17:38:47 INFO  All tests successfuly completed
```

cal_GLAT1751_GLAT1748_20050111_150903

15:09:19 ,bias_voltage,dvm_current,read_current
15:09:19 ,44.8261800977,0.45,0.5803709689
15:09:30 ,89.6162271062,0.89,1.16802030214
15:09:39 ,67.21001221,0.67,0.874951279657
15:09:39 ,slope_in_mA(dvm)/mA(tem),intercept_in_mA(dmv)
15:09:39 ,0.748744200114,0.0152624934184
15:09:39 ,,,,,bias_voltage_(V),current_read_by_tem_(mA),dvm_extapolated_current
15:09:43 ,,,,,0.542181318681,5.04662680457,3.79389504348
15:09:47 ,,,,,7.89267521368,3.62639062463,2.73050144095
15:09:50 ,,,,,15.2919426129,2.18836960425,1.65379154231
15:09:54 ,,,,,22.6910866911,0.773610333022,0.594498743417
15:09:58 ,,,,,25.0602087912,0.332108621226,0.263926897369
15:10:02 ,,,,,25.0586672772,0.332084440614,0.263908792276
15:10:05 ,,,,,25.535981685,0.336860111566,0.267484548203
15:10:09 ,,,,,29.7599151404,0.390130000718,0.307370068747
15:10:13 ,,,,,33.9542515263,0.439373817903,0.344241091255
15:10:17 ,,,,,38.1581452991,0.497225933108,0.387557526979
15:10:21 ,,,,,42.3532216117,0.548899901841,0.426248111365
15:10:24 ,,,,,46.5534774115,0.604491129785,0.467871720865
15:10:28 ,,,,,50.7462106227,0.658450166391,0.508273236568
15:10:32 ,,,,,54.939498779,0.713340156575,0.549371798362
15:10:36 ,,,,,59.1324786325,0.772280399339,0.593502963285
15:10:40 ,,,,,63.3255818071,0.823942277766,0.632184495124
15:10:43 ,,,,,67.5256526252,0.879932485815,0.674106838664
15:10:47 ,,,,,71.7448998779,0.931799899447,0.712942263796
15:10:51 ,,,,,75.965503663,0.983352965118,0.751542322715
15:10:55 ,,,,,80.1587301587,1.04144688645,0.795039809372
15:10:58 ,,,,,84.3518333333,1.0999760588,0.838863187709
15:11:02 ,,,,,88.5572069597,1.15756218727,0.881980467406

basic_20050111_173518

01/11/05 17:36:01 INFO Test Over: All tests Successful

```
17:41:55  default tem status 0xb0000
17:41:55  running temConfigTest
17:41:55  redundant GEM test missing in temConfigTest
17:41:55  entering temConfigParity test
17:41:55  entering tkr tack parity bit test
17:41:57  entering tkr internal parity bit test
17:41:59  entering tkr token parity bit test
17:42:01  entering temCalInternalParityTest
17:42:01  entering temResponseParity test
17:42:01  entering temConfigTrigBufTest test
17:42:03  temConfigCableConTimeoutTest does not exist yet
17:42:03  done with subtest(s), found 0 errors; total errors: 0
17:42:05  functional test(s) interrupted, found 0 total errors
17:42:08  default tem status 0xb0000
17:42:08  running temConfigTest
17:42:08  redundant GEM test missing in temConfigTest
17:42:08  entering temConfigParity test
17:42:08  entering tkr tack parity bit test
17:42:11  entering tkr internal parity bit test
17:42:13  entering tkr token parity bit test
17:42:15  entering temCalInternalParityTest
17:42:15  entering temResponseParity test
17:42:15  entering temConfigTrigBufTest test
17:42:17  temConfigCableConTimeoutTest does not exist yet
17:42:17  done with subtest(s), found 0 errors; total errors: 0
17:42:19  running temDatamasksTest
17:42:20  entering temDatamasksDiag test
17:42:21  entering temDatamasksCal test
17:42:22  entering temDatamasksTkr test
17:42:23  done with subtest(s), found 0 errors; total errors: 0
17:42:25  running temStatusTest
17:42:25  entering temConstatComParity test
17:42:25  entering temConstatPrimaryParity test
17:42:25  entering temConstatComPrefixParity test
17:42:25  entering temConstatTrigMessParity test
17:42:25  entering temConstatTag test
17:42:33  entering temConstatCable test
17:42:39  entering temConstatTimeout test
17:42:40  entering temConstatComParity test
17:42:40  entering temConstatRedundantParity test
17:42:40  entering temConstatRedundantSelected test
17:42:40  entering temConstatEventsSent test
17:42:43  done with subtest(s), found 0 errors; total errors: 0
17:42:45  running temComrespStatTest
17:42:45  entering temComrespStatTest test
17:42:45  takes a few minutes as stands
17:43:21  done with subtest(s), found 0 errors; total errors: 0
17:43:23  running temCaltrgseqTest
17:43:23  entering cal TrigSeq test
17:43:24  done with subtest(s), found 0 errors; total errors: 0
17:43:26  running temTkrtrgseqTest
17:43:26  entering gtccTrgSeqTack test
17:43:27  done with subtest(s), found 0 errors; total errors: 0
17:43:29  running temAddressTest
17:43:29  entering temAddress test
17:43:29  done with subtest(s), found 0 errors; total errors: 0
17:43:31  running gticPowerSupplyControlTest
17:43:31  entering gticPowerSupplyControl test
17:43:42  done with subtest(s), found 0 errors; total errors: 0
17:43:44  running gticConstatComParityTest
17:43:44  entering gticConstatComParity test
17:43:44  done with subtest(s), found 0 errors; total errors: 0
17:43:46  running gticInputmaskTest
```

```
17:43:46  gticInputmask test does not exist
17:43:46  done with subtest(s), found 0 errors; total errors: 0
17:43:48  running gcccConfigTest
17:43:48  entering ccConfigFifoFullCond test
17:43:48  entering Cal sum subtest
17:43:50  entering Cal err subtest
17:43:51  entering Cal data subtest
17:43:54  entering Cal diag subtest
17:43:55  done with subtest(s), found 0 errors; total errors: 0
17:43:57  running gcccLayermaskTest
17:43:57  entering gcccLayermaskTest
17:44:14  done with subtest(s), found 0 errors; total errors: 0
17:44:16  running gcccConfigTest
17:44:16  entering ccConfigFifoFullCond test
17:44:16  entering Cal sum subtest
17:44:18  entering Cal err subtest
17:44:20  entering Cal data subtest
17:44:22  entering Cal diag subtest
17:44:24  done with subtest(s), found 0 errors; total errors: 0
17:44:26  running gcccLatstatFifoTest
17:44:26  entering gcccLatstatFifo test
17:45:53  done with subtest(s), found 0 errors; total errors: 0
17:45:55  running gcccTimeoutTest
17:45:55  entering gcccTimeout test
17:45:58  done with subtest(s), found 0 errors; total errors: 0
17:46:00  running gcccTrgalignTest
17:46:00  gcccTrgalign test does not exist: probably a scope test
17:46:00  done with subtest(s), found 0 errors; total errors: 0
17:46:02  running gcccConfigTest
17:46:02  entering ccConfigFifoFullCond test
17:46:02  entering Cal sum subtest
17:46:03  entering Cal err subtest
17:46:05  entering Cal data subtest
17:46:07  entering Cal diag subtest
17:46:09  done with subtest(s), found 0 errors; total errors: 0
17:46:11  running gtccInputmaskTest
17:46:11  entering gtccInputmaskTest
17:46:20  done with subtest(s), found 0 errors; total errors: 0
17:46:22  running gtccConfigTest
17:46:22  entering gtccConfigCableLength test
17:46:23  entering ccConfigFifoFullCond test
17:46:23  entering tkr sum subtest
17:46:25  entering tkr diag subtest
17:46:54  entering tkr tot subtest
17:46:57  entering tkr err subtest
17:46:59  entering tkr data subtest
17:47:01  done with subtest(s), found 0 errors; total errors: 0
17:47:03  running gtccLatstatFifoTest
17:47:03  entering gtccLatstatFifo test
17:47:12  n.b.: in gtccLatstatFifo; it is not possible to test data fifo write full
bits
17:48:18  done with subtest(s), found 0 errors; total errors: 0
17:48:20  running gtccTimeoutTest
17:48:20  entering gtccTimeout test
17:48:41  done with subtest(s), found 0 errors; total errors: 0
17:48:43  running gtccTrgalignTest
17:48:43  gtccTrgalign test does not exist: probably a scope test
17:48:43  done with subtest(s), found 0 errors; total errors: 0
17:48:45  done with functional test(s), found 0 total errors
```

cal_basic_20050112_082135

01/12/05 08:28:08 INFO Test Over: All tests Successful

tps_1751_1748_20050111_165709

```
16:57:10  TPS calibration data for TPS 1751
16:57:10  please wait approx. 30 sec for the system to settle
16:57:35  dv -0.009015: current 0.130000
16:57:40  dv -0.003863: current 0.464000
16:57:45  dv 0.000395: current 0.742000
16:57:50  dv 0.005659: current 1.082000
16:57:50  slope,intercept

16:57:50  64.908112,0.715246
```

tkr_basic_20050112_083810

01/12/05 08:39:25 INFO Test Over: All tests Successful

bias_1751_1748_20050111_170902

```
17:09:02  reading input file
V:\GLAST\Electronics\TEMPROD\TpsCalibTest\data\cal_1751_1748_20050111_150903.csv
17:09:02  using slope 0.748744 and intercept 0.000015
17:09:02  reading input file
V:\GLAST\Electronics\TEMPROD\TpsCalibTest\data\tkr_1751_1748_20050111_152936.csv
17:09:02  using slope 0.959277 and intercept 0.000009
17:09:02  reading input file
V:\GLAST\Electronics\TEMPROD\TpsCalibTest\data\tps_1751_1748_20050111_165709.csv
17:09:02  using slope 64.908112 and intercept 0.715246
17:09:07

--- Testing MidRange Range ---

17:09:07  Pdu TEM voltage 0: Raw  2784   Calibrated  3.399 V:   tolerance 3.25-3.45
V      result: ok
17:09:07  Pdu TEM voltage 1: Raw  2784   Calibrated  3.399 V:   tolerance 3.25-3.45
V      result: ok
17:09:07  TEM              : Raw  2793   Calibrated  3.410 V:   tolerance 3.25-3.45
V      result: ok
17:09:07  Cal Digital      : Raw  2724   Calibrated  3.326 V:   tolerance 3.25-3.45
V      result: ok
17:09:07  Cal Analog       : Raw  2768   Calibrated  3.379 V:   tolerance 3.25-3.45
V      result: ok
17:09:07  Tkr Digital      : Raw  2940   Calibrated  2.692 V:   tolerance 2.35-2.73
V        result: ok
17:09:07  Tkr Analog A     : Raw  2069   Calibrated  1.585 V:   tolerance 1.3-1.6 V
      result: ok
17:09:07  Tkr Analog B voltage is 2.750916 for MidRange test: out of tolerance range
2.350000-2.730000
17:09:07  Tkr Analog B     : Raw  3004   Calibrated  2.750 V:   tolerance 2.35-2.73
V      result: high
17:09:07  Cal Bias  1      : Raw   775   Calibrated  47.79 V:   tolerance 45.0-55.0
V      result: ok
17:09:07  Cal Bias  0      : Raw   725   Calibrated  44.74 V:   tolerance 40.0-55.0
V      result: ok
17:09:07  Cal Bias Current is 0.000463 for MidRange test: out of tolerance range
0.000500-0.001000
17:09:07  Cal Bias Current :             Calibrated  0.000463 A: tolerance
0.0005-0.001 A  result: low
17:09:07  Tkr Bias  1      : Raw  1287   Calibrated  79.41 V:   tolerance 70.0-85.0
V      result: ok
17:09:07  Tkr Bias  0      : Raw  1124   Calibrated  69.31 V:   tolerance 60.0-75.0
V      result: ok
17:09:07  Tkr Bias Current :             Calibrated  0.001908 A: tolerance
0.0015-0.0025 A    result: ok
17:09:07  Tower 28V V1     : Raw  3390   Calibrated  27.36 V:   tolerance 26.0-28.0
V      result: ok
17:09:07  Tower 28V V2     : Raw  3399   Calibrated  27.43 V:   tolerance 26.0-28.0
V      result: ok
17:09:07  Current Calculation: I=64.908*(2.5/4095)*(V2-V1)+0.715
17:09:07  Tower Current    :             Calibrated  1.07263 A: tolerance 0.9-1.3 A
result: ok
```