SIB FLIGHT CARD

TEST RESULTS DOCUMENTATION PACKAGE

SN GLAT2206

04 OCT 2005

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(Click on link)

TRAVEL)

SILVER ENGINEERING INC.

HIGH RELIABILITY PRODUCTION TEST)

TRAVELER APPROVAL

ENG QA PURCH ASSY DATE 9/15/03

MGR. RELEASE/SHIP TO: DATE

REV	ASSEMBLY NAME	PROCEDURE	ASSY NO.	DRAWING NO.	BOARD & SERIAL NO.	CONTRACT NO.
-	GIAST SIB-REV S1				LAT-DS-01674 Rev S6 SN GLAT 2206	

ITEM	PRODUCTION OPERATION	PARTS VERIFICATION	OPERATOR/ INSPECTOR	DATE START	DATE FINISH	REMARKS	REFERENCE DESIGNATORS
1	Receiving		JC	10/3/05	10/3/05	colored tcladrop markers noted in pictures	
2	Incoming inspection		JC	10/3/05	10/3/05	Blue on all 3 Dots of Humidity Indicator	
						Vias, test points, J1 solder filled on Board side near J2-5, P1 \ No Board marking + peeling on connector taped marking	
3	Connector Alignment		DLS/JC	10/3/05	10/3/05	Alignment looks good / But J5 edge looks melted (no repair recommended)	
4	Test Procedure SIB Flight	Card	JC/S	10/3/05	10/3/05	Demated	
5	Boxed		DLS/JC	10/3/05	10/3/05		
6	Unboxed		JC	10/4/05	10/4/05		
7	Plugged into Chasis for		JS/JC	10/4/05	—	Remate	
	a second Readonly Test of	Memory		—	10/4/05		

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TEST PROCEDURE
SIB FLIGHT CARD
LAT-TD-01678 REV 52
12 JULY 2005

Card Assembly Number	LAT-DS-01674 Rev 56
Card Serial Number	SN GLAT2206
FPGA Label	LAT-DS-03891-52
Test Conductor 1	Dennis Silver
Test Conductor 2	Janet Clifford
Quality Assurance	Janet Clifford
Date of Test	03 OCT 2005

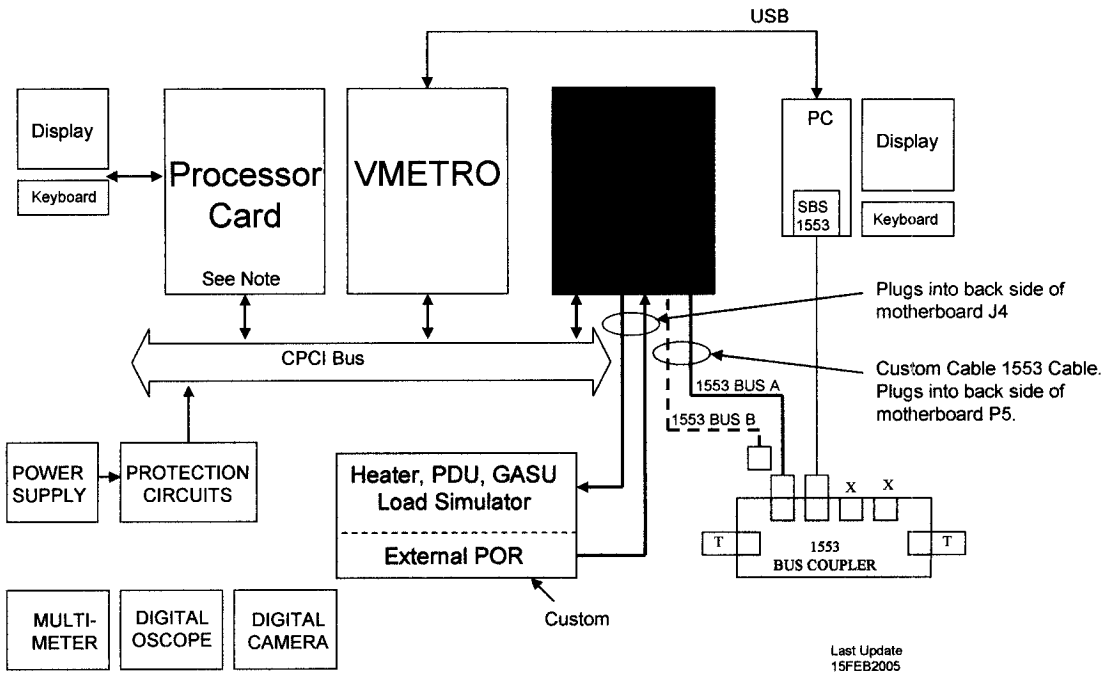
This test procedure shall be used at SEI to test the Flight SIB cards. This procedure assumes the Test Conductors are familiar with the following equipment and software:

VMETRO CPCI emulator
Busview software and scripts
SIB Basics
SBS PCI 1553 card configured as bus controller with PC software
Digital Scope operation
Voltmeter operation

Summary of the tests are as follows:

I. Review and verification of ESD requirements and equipment
II. Continuity testing for card shorts between planes
III. Test fixture power supply test
IV. Verifying voltages on card after power up
V. Verify Actel power switch
VI. Setup and verification of configuration registers
VII. Control/Status Register Test
VIII. EEPROM Unlock Test and Simple EEPROM Write Test
IX. Heater/PDU/GASU test
X. Lower/Upper EEPROM testing:
XI. Lower/Upper EEPROM POR circuit test
XII. SRAM test
XIII. Summit 1553 test, A Bus and B Bus
XIV. 1553 Interrupt test
XV. 1553 SRAM Burst test
XVI. Upper/Lower POR circuit test
XVII. Comprehensive EEPROM Write/Read test

Appendix A Custom 1553 Cable
Appendix B Heater PDU GASU Load Simulator and External POR Generator



Note: Processor Card only installed during Comprehensive EEPROM test.

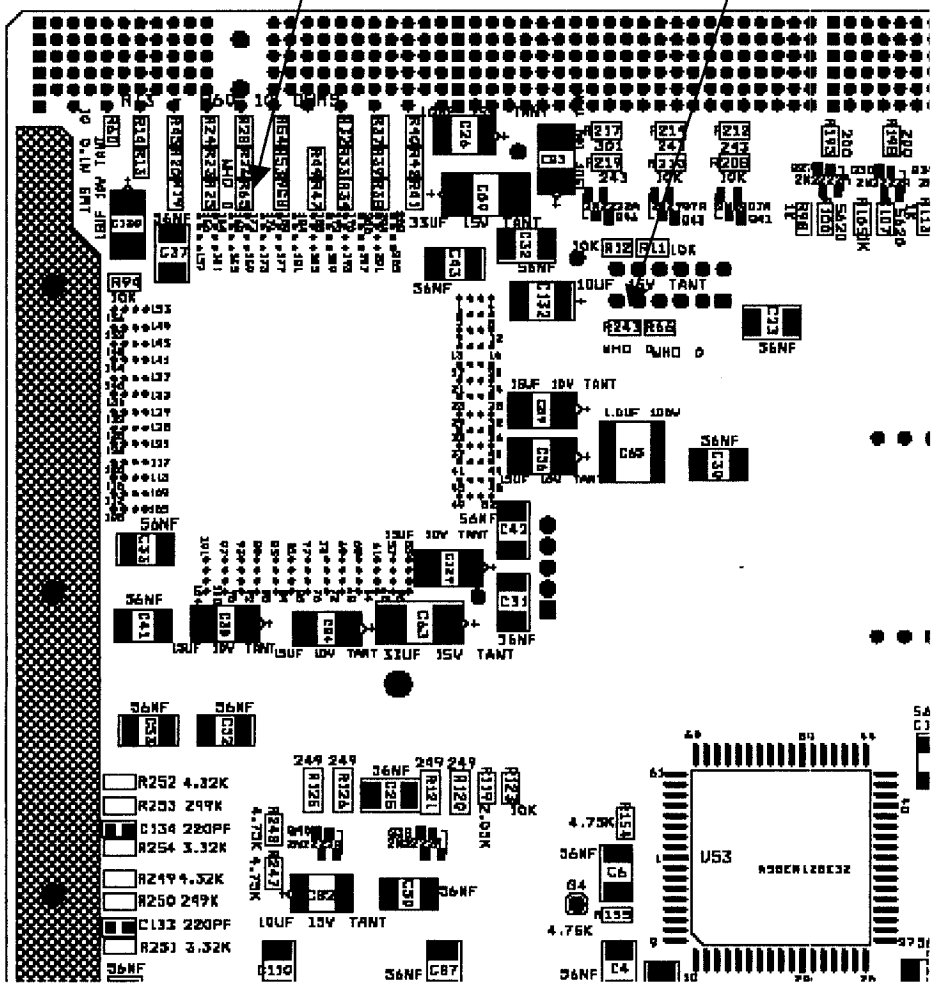
FIGURE 1, Test Configuration

TEST PROCEDURE

Review and verification of ESD requirements and equipment, basic setup

1. Review ESD precautions ✓
2. Test ESD equipment ✓
3. Take pictures of card ✓
4. Visual inspection of card ✓ U1A'S & Testpoints & J1 are solder filled, LOTS OF grainy solder joints at Transistor,
5. Verify R65 (zero ohm) is **NOT** installed ✓
6. Verify R66 and R243 (zero ohm) are both installed ✓ ✓
7. Visual inspection of Capacitor Polarity ✓
8. Visual inspection of SIB CPCI connectors ✓ Alignment on conn good! Still OK!
9. Visual inspection of Test Fixture connectors ✓ ↑ Little off, took Pics

BOTTOM SIDE R65 R66, R243



TC DTd Date 03 OCT 05 QA JC Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

Continuity testing for card shorts between planes

10. Check for shorts by using ohmmeter. Fill in matrix below, use test points as shown in Figure 2.

USING TEK 870

RED

GND	OPEN				
5V	OPEN	28K			
3.3V	OPEN	3.8K	32K		
3.3V_ ACTEL	OPEN	512	19K	4.3K	
+2.5	OPEN	237	23.5	4K	.7K
	CHASSIS GND	GND	5V	3.3V	3.3V_ ACTEL

BLACK

11. All open? Yes If no, then problem.

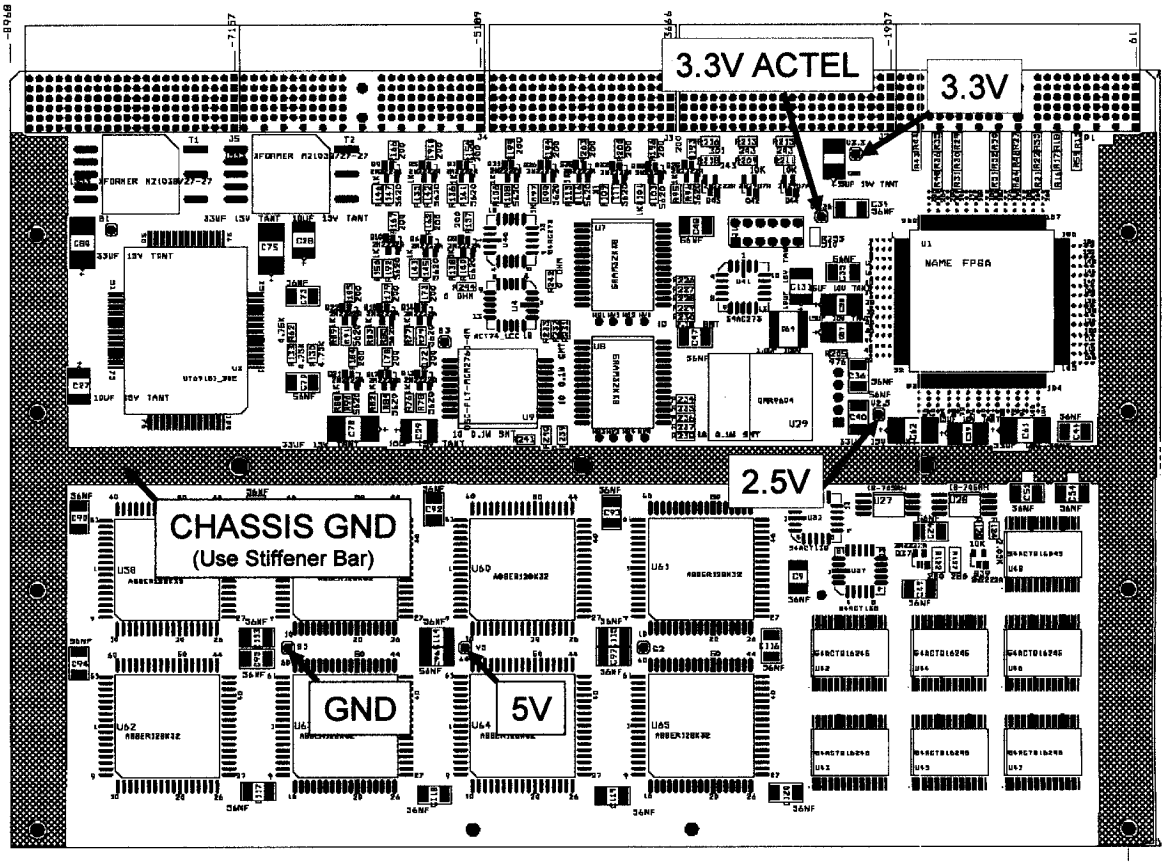


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FIGURE 2, VOLTAGE TEST POINTS

Test fixture power supply test

12. Turn on Test Fixture (no Flight Card Installed) ✓

13. Verify CPCI test fixture power supplies with DVM

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	5.067	—
3.3V	3.135	3.465	3.3266	—
+12	11.4	+12.6	+12.053	—
-12	-11	-13	-11.445	—

.0007 volts @ 50 millions

14. Record 3.3V _____ mA and 5V _____ mA currents ✓

.0015 volts @ 50 millions

15. Turn off power supply ✓

Verifying voltages on card after power up

16. Install SIB into test fixture ✓

17. Connect 1553 cable to channel a (channel a can be live, but should not be running) ✓

18. Turn on power supply, ✓

19. Observe card for hot components —

20. Verify CPCI test fixture power supplies with DVM

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	+ 5.060 v	Y
3.3V	3.135	3.465	+ 3.320 v	Y
+12	11.4	+12.6	+12.075	Y
-12	-11	-13	-11.466	Y

.001 V @ 50 millions .002 V @ 50 millions

21. Record +3.3V _____ mA and +5V _____ mA currents

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Any Problems this page (y/n) NO If yes, add report

22. Verify SIB <u>on card</u> voltages, reference GND, use test points as shown in Figure 2.

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	5.058v	Y
3.3V	3.135	3.465	3.3161	Y
3.3V_ ACTEL	3.135	3.465	3.3073v	Y
+2.5	2.375	2.625	2.5031v	Y

23. Turn off power supply. ✓

Verify Actel power switch

24. Connect Digital Scope using test points in Figure 2:
- a. Ch 1 2.5V 2v/div
- b. Ch 2 3.3V 2v/div
- c. Ch 3 3.3V_Actel 2v/div
- d. Ch 4 not connected
- e. Trigger Mode Normal, Ch 1 rising, 0.7v
- f. Sweep at 2.5ms/div
- g. ✓

25. Arm scope ✓

26. Turn on power supply ✓
- a. Observe the following waveform traces ✓
  - i. Ch1 rises from 0V to +2.5V
  - ii. Ch2 rises from 0V to +3.3V
  - iii. Ch3 rises +3.3V after Ch 1 reaches +0.7V
- b. Repeat 5 times ✓, ✓, ✓, ✓, ✓
- c. Print or photograph waveforms (1 or more) ✓
- d. Label with current time and date ✓

SN2206 STEP26D.JPG

TC DEF Date 03OCT05 QA JC Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

Setup and verification of configuration registers

27. Run SIB configuration script (*SIB SLOT6 CONFIG.SCR*) ✓

28. Verify that configuration registers as listed below: ✓

08000000	084411aa	✓
08000004	04000002	✓
08000008	ff000006	✓
0800000c	00000000	✓
08000010	22000008	✓
08000014	00000000	✓
08000018	00000000	✓
0800001c	00000000	✓
08000020	00000000	✓
08000024	00000000	✓
08000028	00000000	✓
0800002c	00000000	✓
08000030	00000000	✓
08000034	00000000	✓
08000038	00000000	✓
0800003c	00000100	✓
08000040	00000000	✓
08000044	00000000	✓
08000048	00000200	✓

OK

Control/Status Register Test

29. Run script *"SIB SLOT6 REG TEST.SCR"* ✓

30. Were all responses correct? YES

31. What is the current date and time SKIP

32. Highlight screen dump, copy to Word, save as a file name and print, then attach to this test procedure, add date and time to printed file. 1

SN2206 STEP 32. DOC

TC D-A Date 030105 QA JC Date: 10/3/05

Any Problems this page (y/n) NO If yes, add report

EEPROM Unlock Test and Simple EEPROM Write Test

33. Run script 'SIB EEPROM UNLOCK LOWER.scr" ✓

34. Verify status register ✓
   a. PCI: m 22000000
   b. 22000000 : 00000016 ✓

35. Write a single memory location in lower EEPROM
   a. ***Note, to minimize rewriting the same EEPROM location incase this test is run more than one time, please select a different memory location each time this test or other special testing has been run in the past. The range for the lower is 22800000 to 22AFFFFE. Also each new memory location written should be more than 8 longword address location different.***
   b. Memory address written = 22987264 with value CAFE BABE

36. Read memory location written in previous step and verify data matches ✓

37. Verify status register
   a. PCI: m 22000000
   b. 22000000 : 00000016 ✓

38. Run script 'SIB EEPROM UNLOCK UPPER.scr" ✓

39. Verify status register ✓
   a. PCI: m 22000000
   b. 22000000 : 00000026 ✓

40. Write a single memory location in upper EEPROM
   a. ***Note, to minimize rewriting the same EEPROM location incase this test is run more than one time, please select a different memory location each time this test or other special testing has been run in the past. The range for the lower is 22C00000 to 22EFFFFE. Also each new memory location written should be more than 8 longword address location different.***
   b. Memory address written = 22D87488 with value FOOD FOOD

41. Read memory location written in previous step and verify data matches ✓

42. Verify status register
   a. PCI: m 22000000
   b. 22000000 : 00000026 ✓

43. Write Control Register with 00000000 and verify status register ✓
   a. PCI: m 22000004 00000000
   b. PCI: m 22000000
   c. 22000000 : 00000006 ✓

Heater/PDU/GASU test

44. Run Script "SIB HEATER_PDU_GASU_TEST.scr"___✓___
45. Did script pass?___Yes___

SRAM test

46. Run script *"SIB ZERO RAM.scr"*___✓___
47. Read ram first few locations and verify zero data___✓___

a. PCI: m 22600000
b. 22600000 : 00000000
c. 22600004 : 00000000
d. 22600008 : 00000000
e. 2260000c : 00000000
f. 22600010 : 00000000
g. 22600014 : 00000000
h. 22600018 : 00000000
i. 2260001c : 00000000
j. 22600020 : 00000000
k. 22600024 : 00000000

48. Run script "*SIB sram walk test.scr*"___✓___
49. Run script "*SIB sram dumpwalk test.scr*", verify walking 1's, then 0's___✓___
50. Run script *"SIB ZERO RAM.scr"*___✓___

a. PCI: m 22600000
b. 22600000 : 00000000
c. 22600004 : 00000000
d. 22600008 : 00000000

Summit 1553 test, A Bus and B Bus

51. Setup Summit for 1553 test

a. Connect up 1553 Bus A Bus Coupler and wiring to Test PC SBS card ✓

b. Run *script "SIB 1553 descriptor block init testds.scr"* ✓

c. Read SRAM ✓

i. PCI: m 22608100
ii. 22608100 : 00000000
iii. 22608104 : 00000000
iv. 22608108 : 00000000 ✓
v. 2260810c : 00000000
vi. 22608110 : 00000000
vii. 22608114 : 00000000

d. Read SRAM_____

i. PCI: m 22608000
ii. 22608000 : 00000000
iii. 22608004 : 00000000
iv. 22608008 : 00000001
v. 2260800c : 00000002
vi. 22608010 : 00000004
vii. 22608014 : 00000008 ✓
viii. 22608018 : 00000010
ix. 2260801c : 00000020
x. 22608020 : 00000040
xi. 22608024 : 00000080
xii. 22608028 : 00000100
xiii. 2260802c : 00000200

e. Read SRAM_____

i. PCI: m 22608800
ii. 22608800 : 00000000
iii. 22608804 : 00000000
iv. 22608808 : 0000fffe ✓
v. 2260880c : 0000fffd
vi. 22608810 : 0000fffb
vii. 22608814 : 0000fff7 ✓
viii. 22608818 : 0000ffef
ix. 2260881c : 0000ffdf
x. 22608820 : 0000ffbf
xi. 22608824 : 0000ff7f
xii. 22608828 : 0000feff

52. Run SBS Pass 3200 (1553 PC controller software) ✓

53. Connect Remotely = NO ✓

54. Using the pull down menu, >PROJECT >LOAD SETUP > SIB_SETUP.ASU ✓

55. Screen should look like this ✓

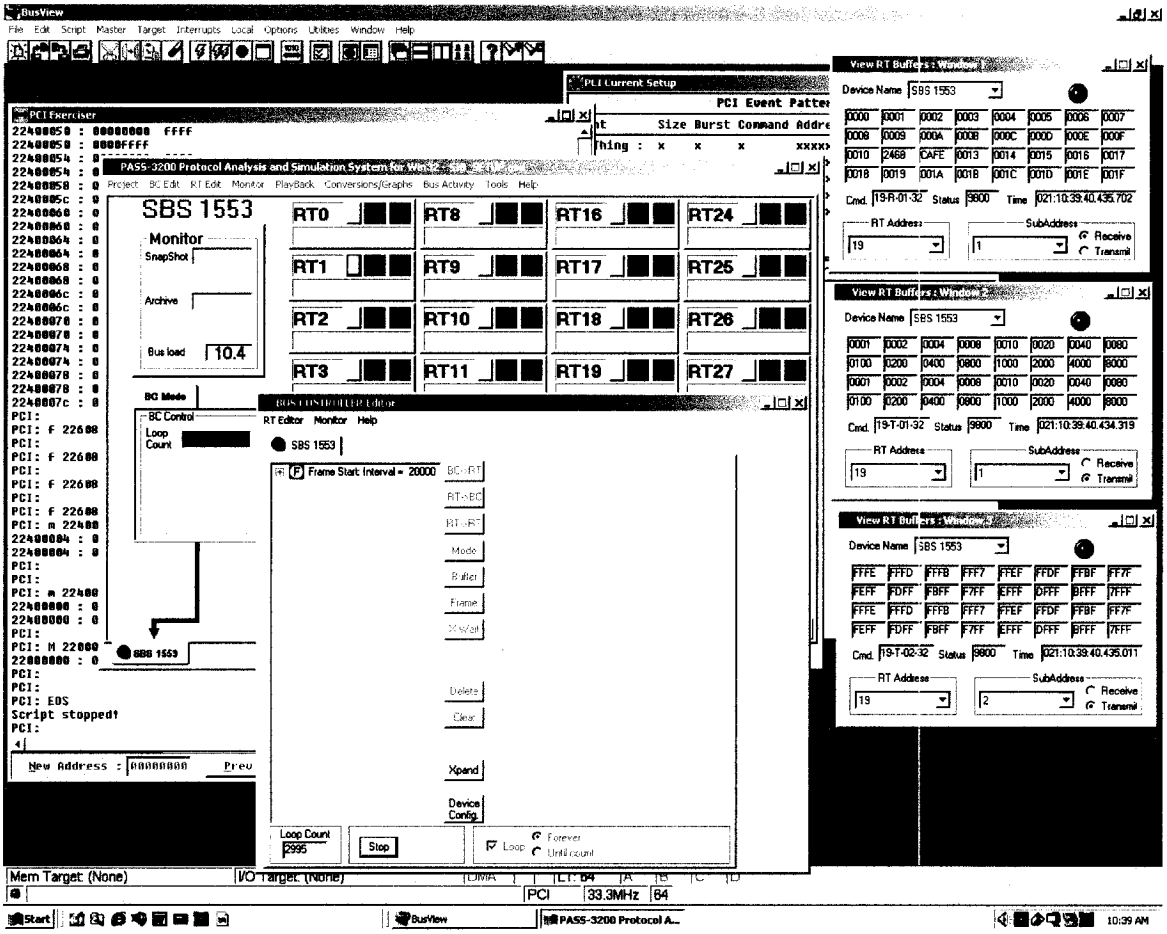

FIGURE 3, SBS 1553 PC SCREEN

56. If SBS software fails to load setup, then it can be configured by running steps (58-61). If SBS software loads ok, you can skip steps58-61.

57. Can you skip steps 58-61? YES

58. Select BC Edit_____

59. Select RT to BC_____

a. Select RT Address 19
b. Select RT Sub Address 1
c. Select Word Count 32

SKIP

60. Select RT to BC_____

a. Select RT Address 19
b. Select RT Sub Address 2

TC DAF Date 030c705 QA JC Date: 10/3/05

Any Problems this page (y/n) NO If yes, add report

c. Select Word Count 32

61. Select BC to RT_____
   a. Select RT Address 19
   b. Select RT Sub Address 1
   c. Select Word Count 32
   d. Select Date Buffer 1
   e. Type data FEED in location 1
   f. Type data DEAD in location 2
   g. Type data BEEF in location 3
   h. Type data BABE in location 4
   i. Type data FACE in location 5
   j. Type data CAFE in location 6
   k. Type data 5A5A in location 7
   l. Type data A5A5 in location 8
   m. Type data F0F0 in location 9
   n. Type data 0F0F in location 10
   o. Select BR to end data buffer 1 edit
   p. Select BUS A
   q. Select Continue on Error
   r. Select Loop Forever

SKIP

62. Select RUN ✓
63. Verify Green Monitor Lamp at top of BC Editor Screen ✓
64. Select Main SBS1553 Pass 3200 screen. ✓
   a. Verify that RT 19 is illuminated green ✓
   b. Verify that the Loop Count Indicator is incrementing
65. Select Bus Activity ✓

66. Select Percent Display ✓
   a. Verify that RT 19 is receiving about 33% of the time ✓
   b. Verify that RT 19 is transmitting about 67% of the time ✓
67. Select OK ✓
68. Select Bus Activity ✓
69. Select Bus Count Analysis ✓
   a. Verify that RT 19 CMD Count is incrementing with NO Errors ✓
70. Select OK ✓
71. Select Monitor ✓
72. Select RT Viewers ✓ (three should be already be in view)
73. Select Sub Address 1, Receive ✓
   a. Verify monitor lamp is illuminated green and status=9800
Verify 32 words of data that matches data buffer 1 ✓

74. Select Sub Address 1, Transmit ✓
   a. Verify monitor lamp is illuminated green and status=9800 ✓
   b. Verify 32 words of walking ones data ✓

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Any Problems this page (y/n) NO If yes, add report

75. Select Sub Address 2, Transmit ✓
   a. Verify monitor lamp is illuminated green and status=9800 ✓
   b. Verify 32 words of walking zeros data from FFFE to 7FFF ✓

76. Select Bus View and verify data ✓
   a. PCI: m 22608100
   b. 22608100 : 00000200 (actual data may vary) ✓
   c. 22608104 : 0000862f (actual data may vary) ✓
   d. 22608108 : 0000feed
   e. 2260810c : 0000dead
   f. 22608110 : 0000beef
   g. 22608114 : 0000babe
   h. 22608118 : 0000face
   i. 2260811c : 0000cafe ✓
   j. 22608120 : 00005a5a
   k. 22608124 : 0000a5a5
   l. 22608128 : 0000f0f0
   m. 2260812c : 00000001
   n. 22608130 : 00000002
   o. 22608134 : 00000003

77. At location 22608138 write 7777, hit ENTER, Press P and verify that it returns to the value 4 ✓
   PCI : m 22608138
   a. 22608138 : 00000004 7777 ✓
   b. 22608138 : 00007777 (note, sometimes the data is overwritten to value 4)
   c. 22608134 : 00000003
   d. 22608138 : 00000004 ✓
   e.

78. Select BC Edit then select STOP ✓

79. Remove 1553 Bus cable from A ✓

80. Summit Reset, _____ ✓
   a. PCI: m 22000004
   b. 22000004 : 00000000 80
   c. 22000004 : 00000080 0

81. Run script *"SIB ZERO RAM.scr"* ✓

   a. Connect up 1553 Bus **B** Bus Coupler and wiring to Test PC SBS card ✓

   b. Run *script "SIB 1553 descriptor block init testds.scr"* ✓

c. Read SRAM_____
   i. PCI: m 22608100
   ii. 22608100 : 00000000
   iii. 22608104 : 00000000
   iv. 22608108 : 00000000
   v. 2260810c : 00000000
   vi. 22608110 : 00000000
   vii. 22608114 : 00000000

d. Read SRAM_____
   i. PCI: m 22608000
   ii. 22608000 : 00000000
   iii. 22608004 : 00000000
   iv. 22608008 : 00000001
   v. 2260800c : 00000002
   vi. 22608010 : 00000004
   vii. 22608014 : 00000008
   viii. 22608018 : 00000010
   ix. 2260801c : 00000020
   x. 22608020 : 00000040
   xi. 22608024 : 00000080
   xii. 22608028 : 00000100
   xiii. 2260802c : 00000200

e. Read SRAM_____
   i. PCI: m 22608800
   ii. 22608800 : 00000000
   iii. 22608804 : 00000000
   iv. 22608808 : 0000fffe
   v. 2260880c : 0000fffd
   vi. 22608810 : 0000fffb
   vii. 22608814 : 0000fff7
   viii. 22608818 : 0000ffef
   ix. 2260881c : 0000ffdf
   x. 22608820 : 0000ffbf
   xi. 22608824 : 0000ff7f
   xii. 22608828 : 0000feff

82. Select BC Edit then select RUN _____

83. Verify Green Monitor Lamp at top of BC Editor Screen_____

84. Select Main SBS1553 Pass 3200 screen. _____
   a. Verify that RT 19 is illuminated green
   b. Verify that the Loop Count Indicator is incrementing

85. Select Bus Activity_____

86. Select Percent Display_____
   a. Verify that RT 19 is receiving about 33% of the time
   b. Verify that RT 19 is transmitting about 67% of the time
87. Select OK_____
88. Select Bus Activity_____
89. Select Bus Count Analysis_____
   a. Verify that RT 19 CMD Count is incrementing with NO Errors
90. Select OK_____
91. Select Monitor_____
92. Select RT Viewers_____
93. Select New RT Viewer_____
94. Select RT Address 19_____
95. Select Sub Address 1, Receive_____
   a. Verify monitor lamp is illuminated green and status=9800
   b. Verify 32 words of data that matches data buffer 1
96. Select Sub Address 1, Transmit_____
   a. Verify monitor lamp is illuminated green and status=9800
   b. Verify 32 words of walking ones data
97. Select Sub Address 2, Transmit_____
   a. Verify monitor lamp is illuminated green and status=9800
   b. Verify 32 words of walking zeros data from FFFE to 7FFF
98. Select Bus View and verify data_____
   a. PCI: m 22608100
   b. 22608100 : 00000200 (actual data may vary)
   c. 22608104 : 0000862f (actual data may vary)
   d. 22608108 : 0000feed
   e. 2260810c : 0000dead
   f. 22608110 : 0000beef
   g. 22608114 : 0000babe
   h. 22608118 : 0000face
   i. 2260811c : 0000cafe
   j. 22608120 : 00005a5a
   k. 22608124 : 0000a5a5
   l. 22608128 : 0000f0f0
   m. 2260812c : 00000001
   n. 22608130 : 00000002
   o. 22608134 : 00000003
99. At location 22608138 write 7777, hit ENTER, Press P and verify that it returns to the value 4_____
   a. PCI : m 22608138
   b. 22608138 : 00000004 7777
   c. 22608138 : 00007777 (note, sometimes the data is overwritten to value 4)
   d. 22608134 : 00000003
   e. 22608138 : 00000004

1553 Message Interrupt test

100. Note, 1553 should still be running from previous test ✓

101. Select BC Edit then select STOP ✓

102. Clear possible interrupt in configuration register by writing 300. Read 08000048 multiple time should always be 200 ✓

a. PCI: M 08000048 C
b. 08000048 : 00000300 300
c. 08000048 : 00000200
d. 08000048 : 00000200
e. 08000048 : 00000200
f. 08000048 : 00000200

103. Select BC Edit then select Run ✓

104. Clear possible interrupt in configuration register by writing 300 (several times). Read 02000048 multiple time should always revert back 300 ✓

a. 08000048 : 00000300 300
b. 08000048 : 00000300 300
c. 08000048 : 00000300 300
d. 08000048 : 00000200 Note, sometimes afterwriting 300, it will still be 200, but the next read will be 300
e. 08000048 : 00000300
f. 08000048 : 00000300 300
g. 08000048 : 00000300
h. 08000048 : 00000300

1553 You Fail Interrupt test

105. Select BC Edit then select STOP ✓

106. Clear possible interrupt in configuration register by writing 300. Read 08000048 multiple time should always be 200 ✓

a. PCI: M 08000048 C
b. 08000048 : 00000300 300
c. 08000048 : 00000200
d. 08000048 : 00000200
e. 08000048 : 00000200
f. 08000048 : 00000200

107. Interrupt test, Turn on VMETRO Trace ✓

108. Force YF_INT (You Fail) ✓

a. PCI: M 22400010
b. 22400010 : 00000400 ✓
c. 22400010 : 00000000
d. 22400010 : 00000000 ✓
e. 22400010 : 00000000 1000
f. 22400010 : 00001000

109. Verify Interrupt was received

a. PCI: M 08000048 C
b. 08000048 : 00000300
c. 08000048 : 00000300
d. 08000048 : 00000300 300
e. 08000048 : 00000200
f. 08000048 : 00000200 ✓
g. 08000048 : 00000200
h. 08000048 : 00000200
i. 08000048 : 00000200

110. Halt Trace and Show Trace, verify Interrupt went active, then inactive ✓

111. Select BC Edit then select Run ✓

1553 SRAM BURST TEST

112. Verify 1553 bus is running ok. ✓

113. Run *Script SIB SRAM BURST TEST.scr* ✓

114. Verify 1553 bus is running ok. ✓

115. Run >Script >RUN LOOP 1000 ✓

116. Verify 1553 bus is running ok during loop. ✓
(Reference Figure 3

TC DYA Date 030CT05 QA JC Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

Lower/Upper EEPROM POR Circuit Test

117. Using voltmeter, measure voltages at R249 and R252 probe points. Reference Figure 4.

a. Voltage at R249 1.4658
b. Voltage at R252 1.4680
c. Range should be 1.40V to 1.49V ✓

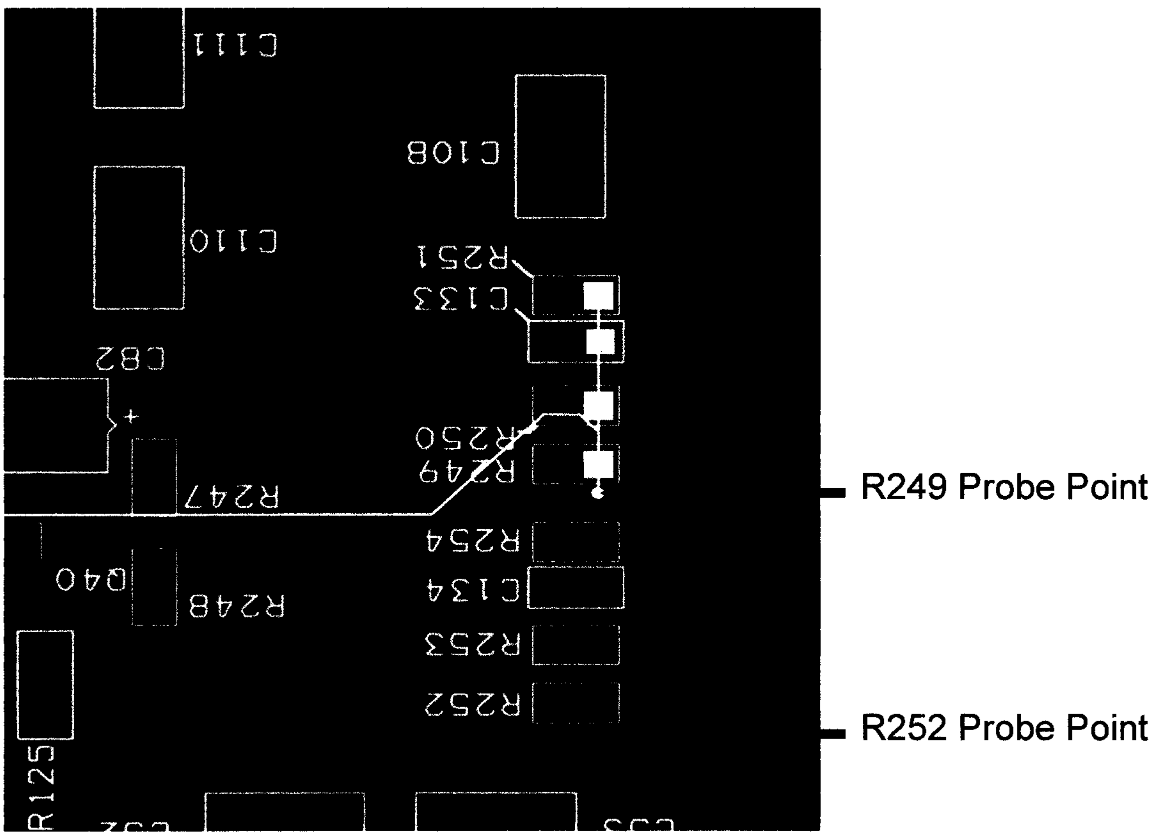


FIGURE 4, POR Probe Points (as viewed from bottom side of CCA in test fixture)

118. Run Script *"SIB POR Mem test.scr"* (*read step a. first*) ✓

a. Note this step does not need to be done if data already exist in memory. Run Script *"SIB POR Mem dump test.scr"* and if data counts up do not run script *"SIB POR Mem test.scr"* ✓

TC DH Date 030105 QA jc Date: 10/3/05

Any Problems this page (y/n) no If yes, add report

119. Verify POR connects to all memory in Upper Bank

a. Run Script "*SIB POR Mem dump test.scr*" ✓
b. Data should increment? ✓
c. Connect or Hold special Test Lead #1 with built in 3.3K resistor to Gnd at R249 Probe Point ✓
d. Run Script "*SIB POR Mem dump test.scr*" ✓
e. Data in address range 22C00000 to 22EFFFC should be all F's and only Lower Address range (22800000 to 22AFFFFC) should ✓ increment ✓
f. Remove Probe ✓

120. Verify POR connects to all memory in Lower Bank

a. Run Script "*SIB POR Mem dump test.scr*" ✓
b. Data should increment? ✓
c. Connect or Hold special Test Lead #1 with built in 3.3K resistor to Gnd at R252 Probe Point ✓
d. Run Script "*SIB POR Mem dump test.scr*" ✓
e. Data in address range 22800000 to 22AFFFC should be all F's and only Upper Address range (22C00000 to 22EFFFFC) should increment ✓
f. Remove Probe ✓
g. Power off test chassis ✓

121. Verify POR works during powerup/power down. Reference probe points in Figure 5.

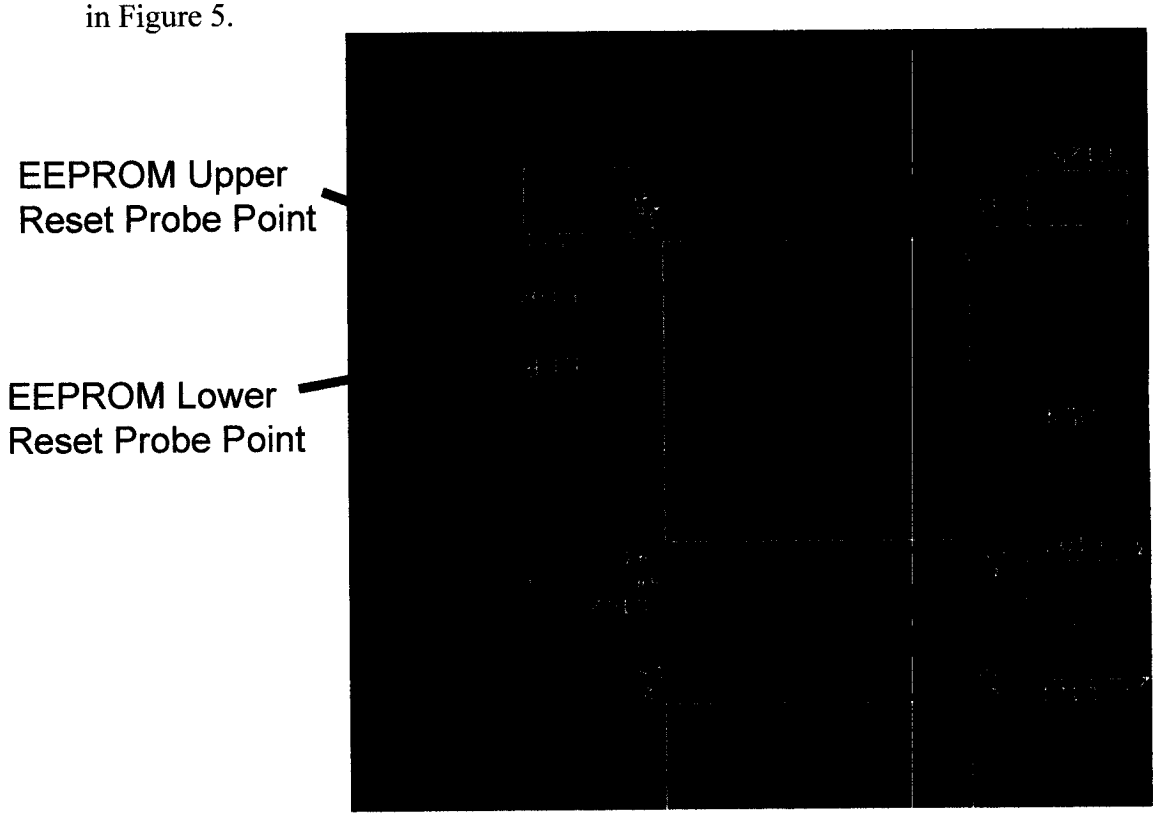


FIGURE 5, Upper and Lower EEPROM Reset Probe Points (as viewed from back side of CCA while in test fixture)

a. Adjust scope
   i. ch 1 = 5v/div, 2, & 3 = 2v/div, ✓ (label scope +5v, EU_RES-, EL_RES-)
   ii. 40ms sweep ✓
   iii. Trigger on Channel 1 Rising ✓

b. Connect Scope leads
   i. Ch 1 to +5V on test chassis
   ii. Ch 2 to EEPROM Upper Reset Probe Point
   iii. Ch 3 to EEPROM Lower Reset Probe Point ✓

c. Adjust scope:
   i. Cycle power on and verify EEPROM Upper and Lower Reset POR lags +5v by appx 180-220ms ✓
   ii. Repeat 5 times ✓, ✓, ✓, ✓, ✓
   iii. Photograph or print waveform (just 1) ✓
   iv. Label Photo/Print with current time and date SN 2206 STEP 121C. JPG

TC DYA Date 03OCT05 QA JC Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

d. Adjust scope: 2v, trig ch 1 falling normal, H40ms, ✓
   i. Cycle power off and verify POR goes low while +5 decays ✓
   ii. Repeat 5 times ✓, ✓, ✓, ✓, ✓
   iii. Photograph or print waveform (just 1) ✓
   iv. Label Photo/Print with current time and date ✓
e. Turn off test fixture

SN220G SEP1210.JPG

TC DYA Date 030CT05 QA JC Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

Comprehensive EEPROM Write/Read test

122. Install Processor card into test chassis and boot system.___✓___
123. Turn off virus protection software___✓___
124. Make sure no screen savers are on___✓___
125. Unplug network cable___✓___
126. Open power point and minimize (to be used for screen capture)___✓___
127. Run GLAST FULL MEM TEST, reference Figure 6

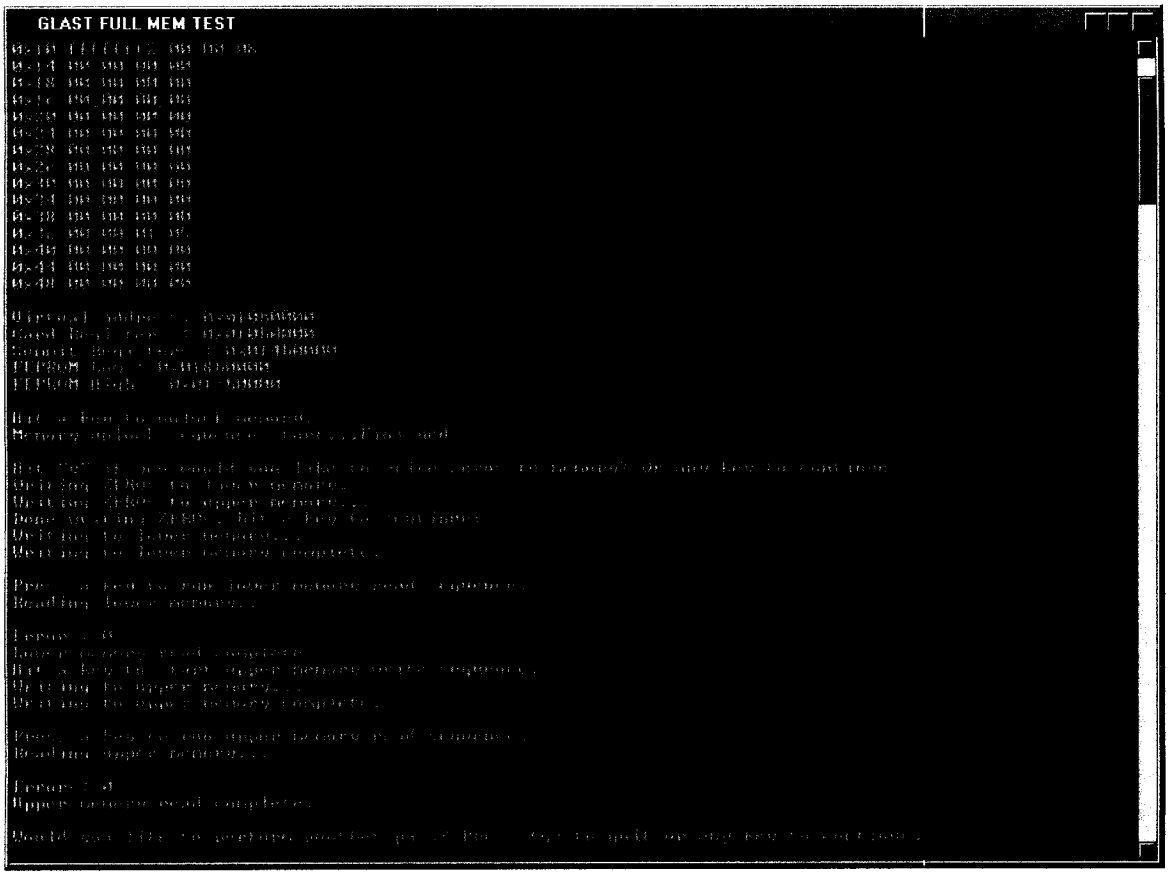


FIGURE 6, GLAST Full Memory Test screen capture.

128. Press any key to unlock memory___✓___
129. Hit "y" to write zeros in memory (this takes 4 minutes) ___✓___
130. Press any key to run lower memory write (this takes 2 minutes)___✓___
131. Press any key to run lower memory read. Any errors?___N___
132. Press any key to run upper memory write (this takes 2 minutes)___✓___
133. Press any key to run upper memory read. Any errors?___N___
134. Save screen capture to power point file and name file with the current date and time ___✓___ SN2206 STEP134.PPT

TC DLS Date 03017/05 QA ___ Date: 10/3/05
Any Problems this page (y/n) NO If yes, add report

135. Press q to quit ✓

136. Run GLAST READ MEM ONLY TEST, reference Figure 7

FIGURE 7, GLAST READ MEM ONLY TEST screen capture

137. Hit any key to run read of upper and lower eeprom 10 times ✓

138. Any Errors reported? NO

139. Capture screen and add to power point file. ✓

140. Close program ✓

141. Remove card, inspect cPCI connectors on text fixture and SIB ✓

142. Take post test pictures of card ✓

143. Attach printouts, photographs, and pertinent information to signed test report. ✓

144. TEST COMPLETE ALL OK

TC DVA Date 03 OCT 05 QA JC Date: 10/3/05

Any Problems this page (y/n) NO If yes, add report

SN2206

SN2206, FLIGHT SIB

① Received 30SEP05

② Box opened 03OCT05

③ SHOCK SENSORS WERE TRIGGERED, took PICS
NOTE, BLACK BOX WAS NOT TAPED CLOSED

④ STARTED Procedure

⑤ Steps 1-11 OK

NOTE J5 connector has some damage, but OK
took PICS

NOTE: FILLED VIAS J1, U1, J2-J5, P1 test points

ALSO SN CABLE ON CONNECTOR IS PEELING OFF

⑥ STEP 12-15 OK

⑦ STEP 16-240K

⑧ STEP 24-121 OK

⑨ STEP 122-144

ALL TEST PASSED 03OCT05

⑩ Re-bagged @ 4:30PM 03OCT05

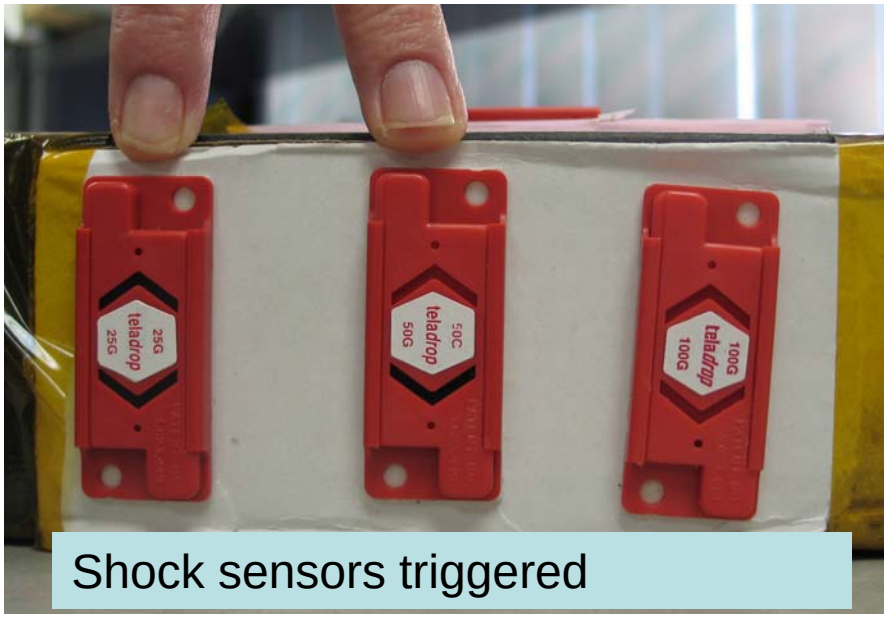
⑪ Reinstalled into chassis, did EEPROM READ ONLY TEST
PASSED OK 04OCT05 1445 PM

CARD WAS POWERED OFF APPX 21hrs

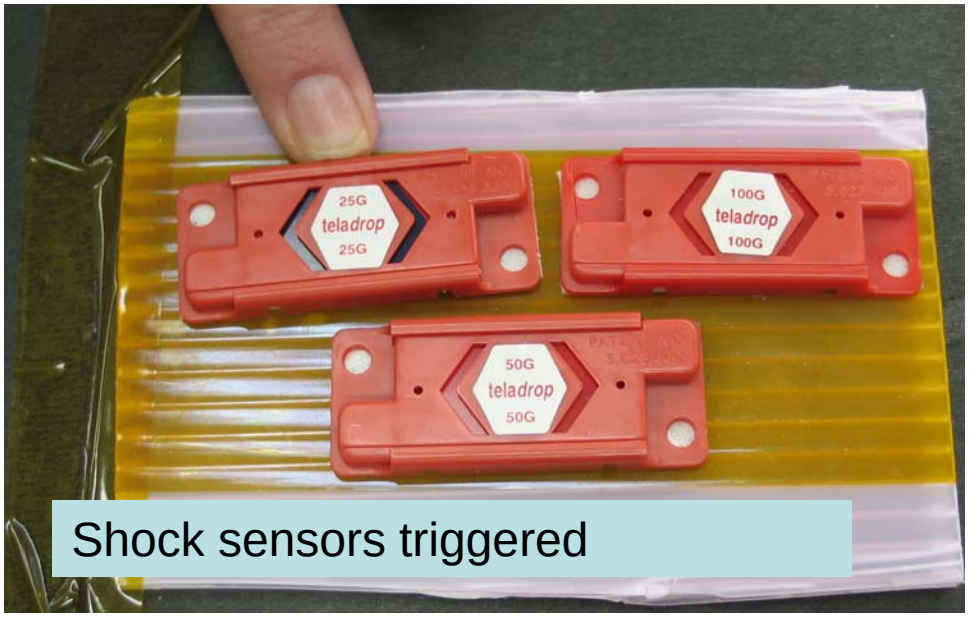
⑫ Rebagged + BOXED !

(END)

SIB SN GLAT2206



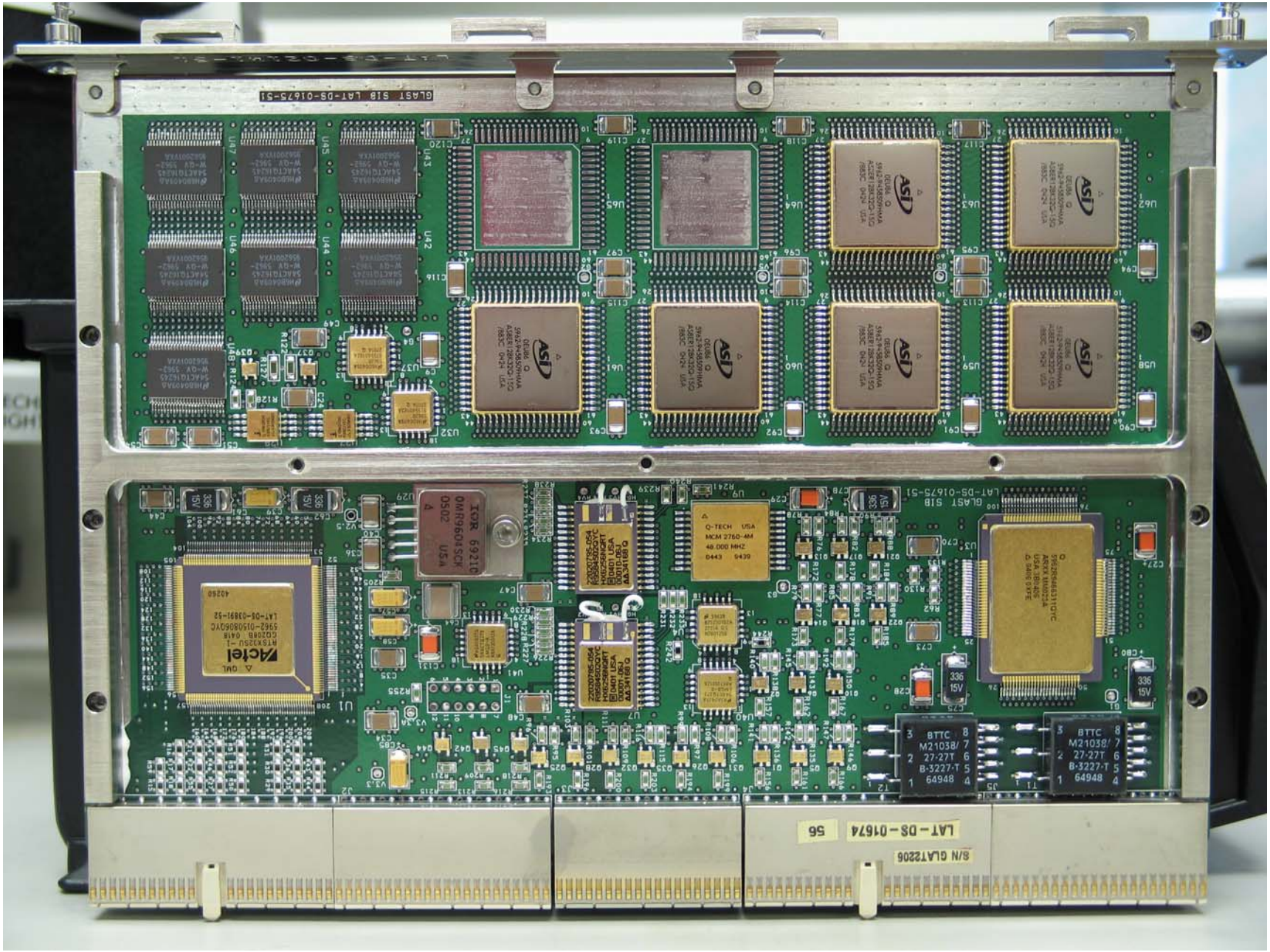
Shock sensors triggered



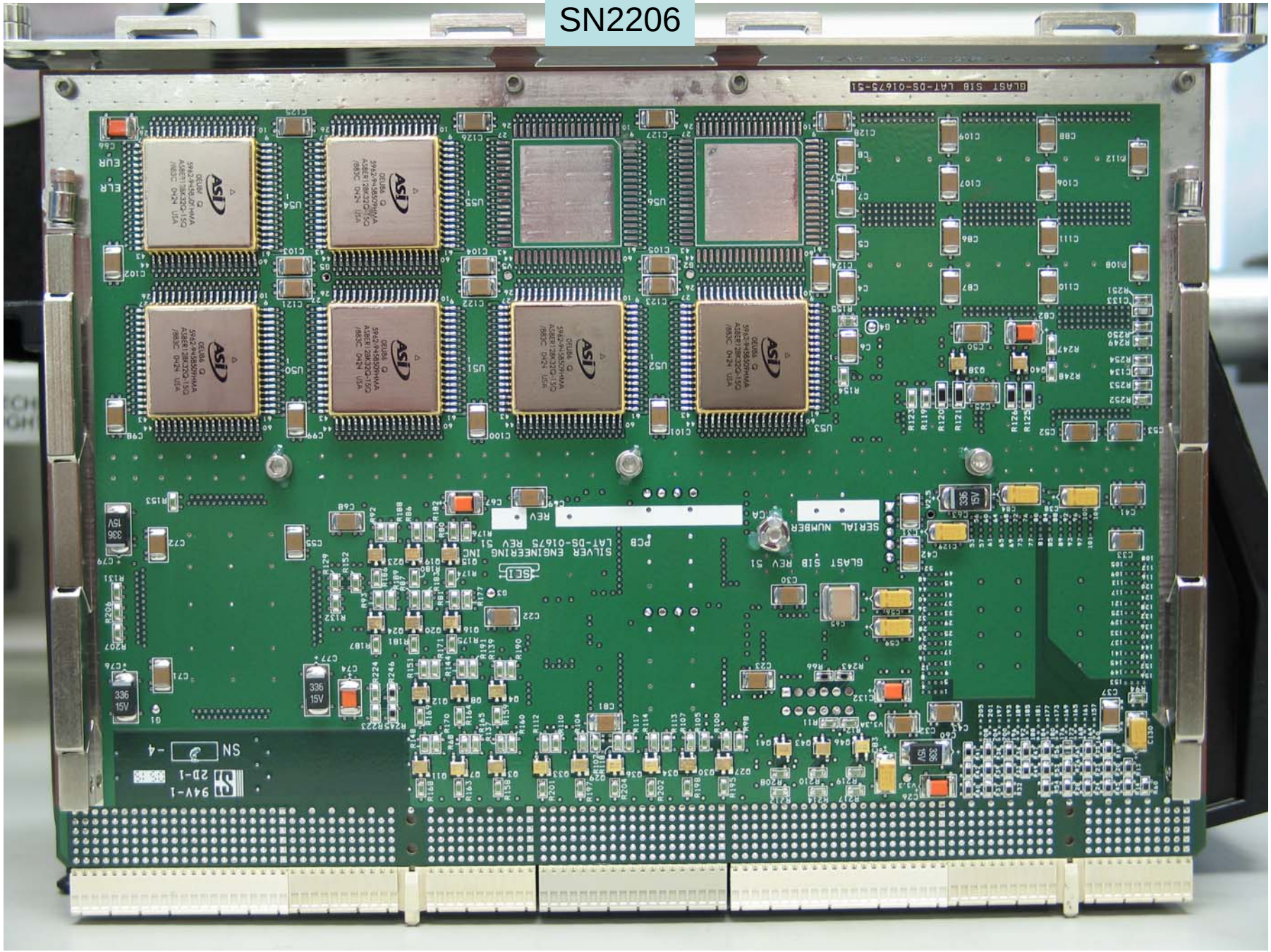
Shock sensors triggered

Box was not taped closed.

SN2206



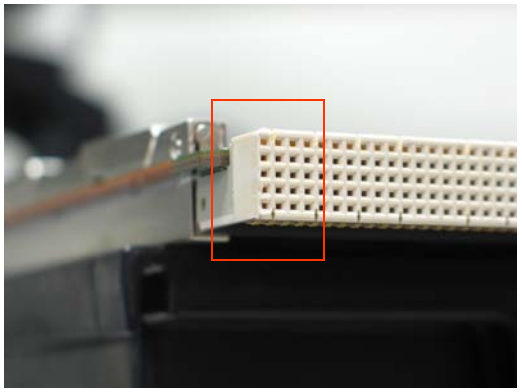
SN2206

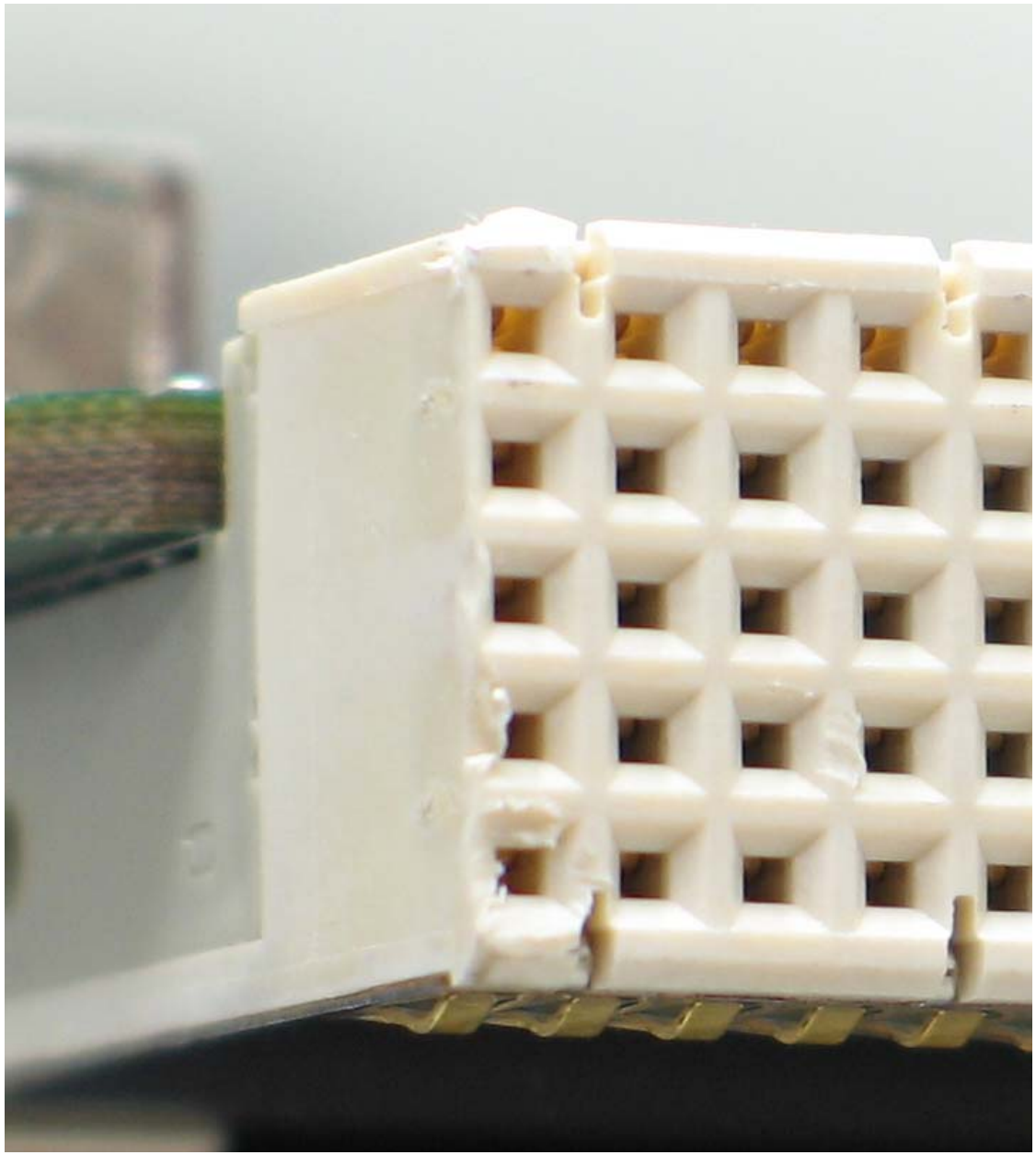

GLAST SIB LAT-DS-01675-S1
SERIAL NUMBER
REV
PCB
LAT-DS-01675 REV S1
SILVER ENGINEERING INC
GLAST SIB REV S1

Workmanship areas of concern for SN2206

1. CPCI Connector J5 minor damage
2. Labels

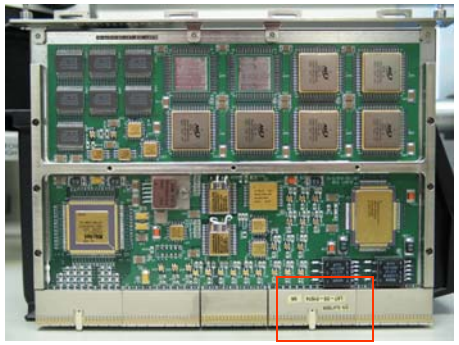
SIB SN GLAT2206

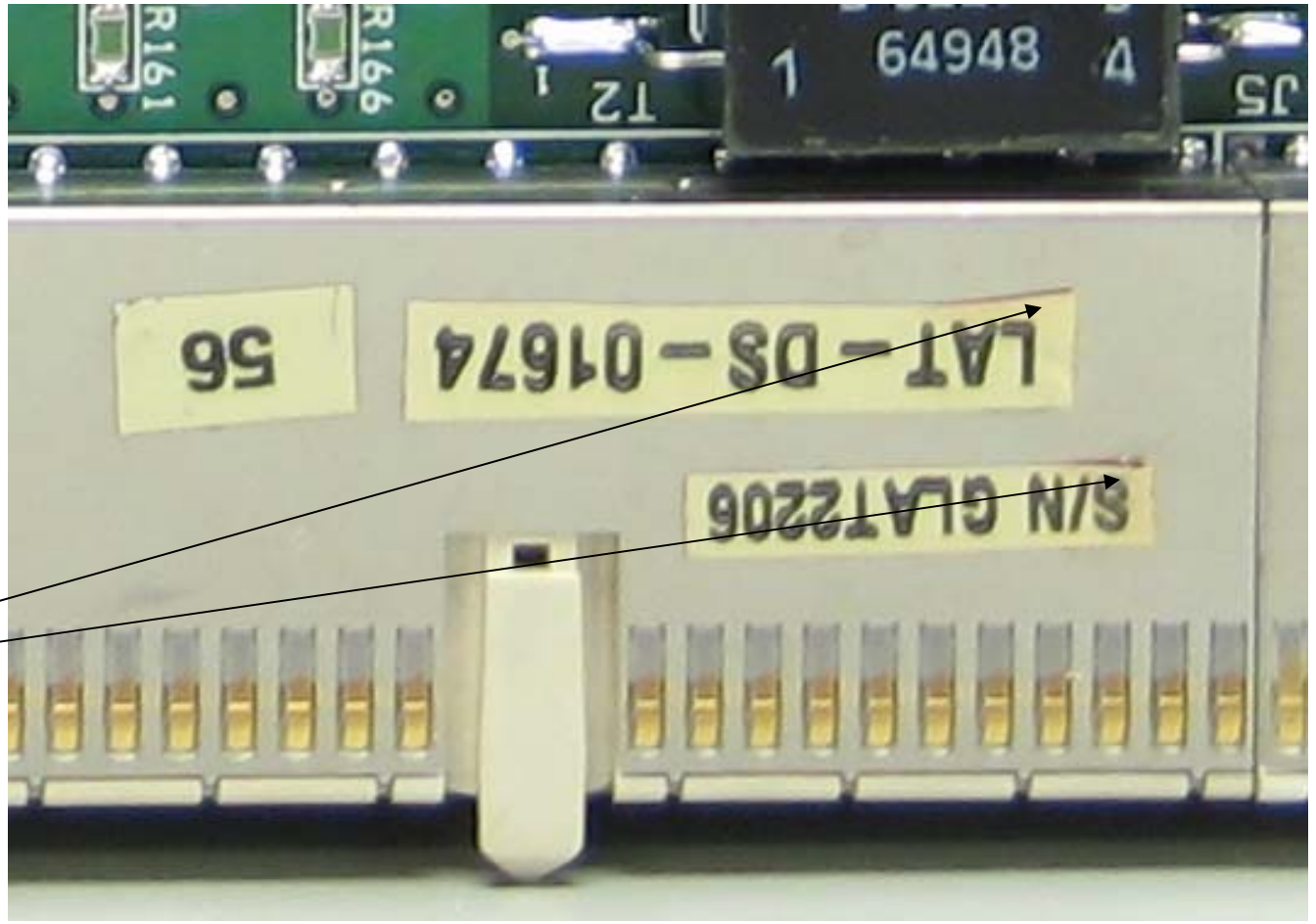




J5 Connector,
Incoming inspection
(card not plugged
into test chassis)

SIB SN GLAT2206





Labels on connector peeling off. Labels are also in a bad place and could come off into backplane.

SCREEN CAPTURE FOR SN2206 TEST PROCEDURE STEP 32

```
PCI:
PCI: dls
Script loaded!
PCI: run 1
PCI:  configuration setup for sib slot 6 card
PCI: w 8000000 c
08000000 :
08000004 : 2
08000008 :
0800000c :
08000010 : 22000000
08000014 : .
PCI:
PCI: w 8000048 c
08000048 : 200
0800004c : .
PCI:
PCI: m 8000000 c
08000000 : 084411aa
08000004 : 04000002
08000008 : ff000006
0800000c : 00000000
08000010 : 22000008
08000014 : 00000000
08000018 : 00000000
0800001c : 00000000
08000020 : 00000000
08000024 : 00000000
08000028 : 00000000
0800002c : 00000000
08000030 : 00000000
08000034 : 00000000
08000038 : 00000000
0800003c : 00000100
08000040 : 00000000
08000044 : 00000000
08000048 : 00000200  .
PCI:
PCI: m 22000000
22000000 : 00000000
22000004 : 00000080  .
PCI:
PCI: m 22000004
22000004 : 00000080  0
22000004 : 00000000  .
PCI:
PCI: m 22000000
22000000 : 00000002
22000004 : 00000000
22000008 : 00000000
2200000c : 00000000
22000010 : 00000002
```

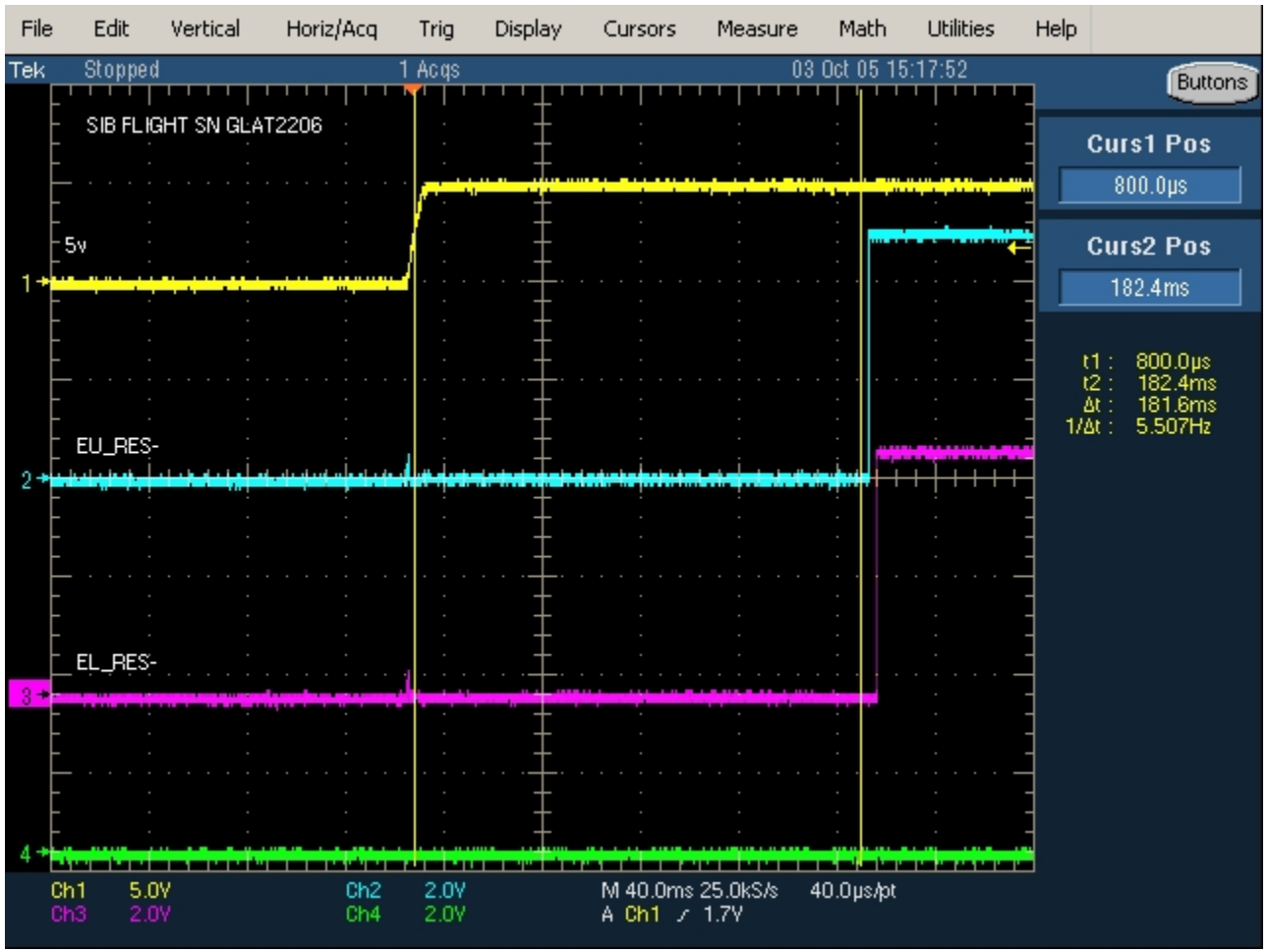
```
22000014 : 00000000  .
PCI:
PCI:
PCI: EOS
Script stopped!
PCI: m 08000000 c
08000000 : 084411aa
08000004 : 04000002
08000008 : ff000006
0800000c : 00000000
08000010 : 22000008
08000014 : 00000000
08000018 : 00000000
0800001c : 00000000
08000020 : 00000000
08000024 : 00000000
08000028 : 00000000
0800002c : 00000000
08000030 : 00000000
08000034 : 00000000
08000038 : 00000000
0800003c : 00000100
08000040 : 00000000
08000044 : 00000000
08000048 : 00000200
0800004c : 00000000
08000050 : 00000000
PCI: dls
Script loaded!
PCI: run 1
PCI: -- SIB REGISTER TEST
PCI: -- TEST WRITTEN 11 JULY 2005
PCI: PAUSE
Press any key to continue...
PCI: -- WATCH DOG TIMMER TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
PCI: M 22000000
22000000 : 00000006
22000004 : 00000000
22000008 : 00000000
2200000c : 00000000
22000010 : 00000006  0
22000010 : 00000002  .
PCI:
PCI: M 22000000
22000000 : 00000002  .
PCI:
PCI: --WAIT 60SEC  ADDRESS 22000000 SHOULD BE = 00000002
PCI: wait 60000
PCI: M 22000000
22000000 : 00000002  .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 00000002
```

PCI: --WAIT 6SEC
PCI: wait 6000
PCI: M 22000000
22000000 : 00000006 .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 00000006
PCI: --END OF WDT TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
PCI:
PCI:
PCI: ----------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: -- SUMMIT RESET TEST
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000000 80
22000004 : 00000080 .
PCI:
PCI: M 22000000
22000000 : 00000004 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 00000004
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000080 0
22000004 : 00000000 .
PCI:
PCI: M 22000000
22000000 : 00000006 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 00000006
PCI: PAUSE
Press any key to continue...
PCI:
PCI: --END OF SUMMIT RESET TEST
PCI:
PCI:
PCI:
PCI: PAUSE
Press any key to continue...
PCI:

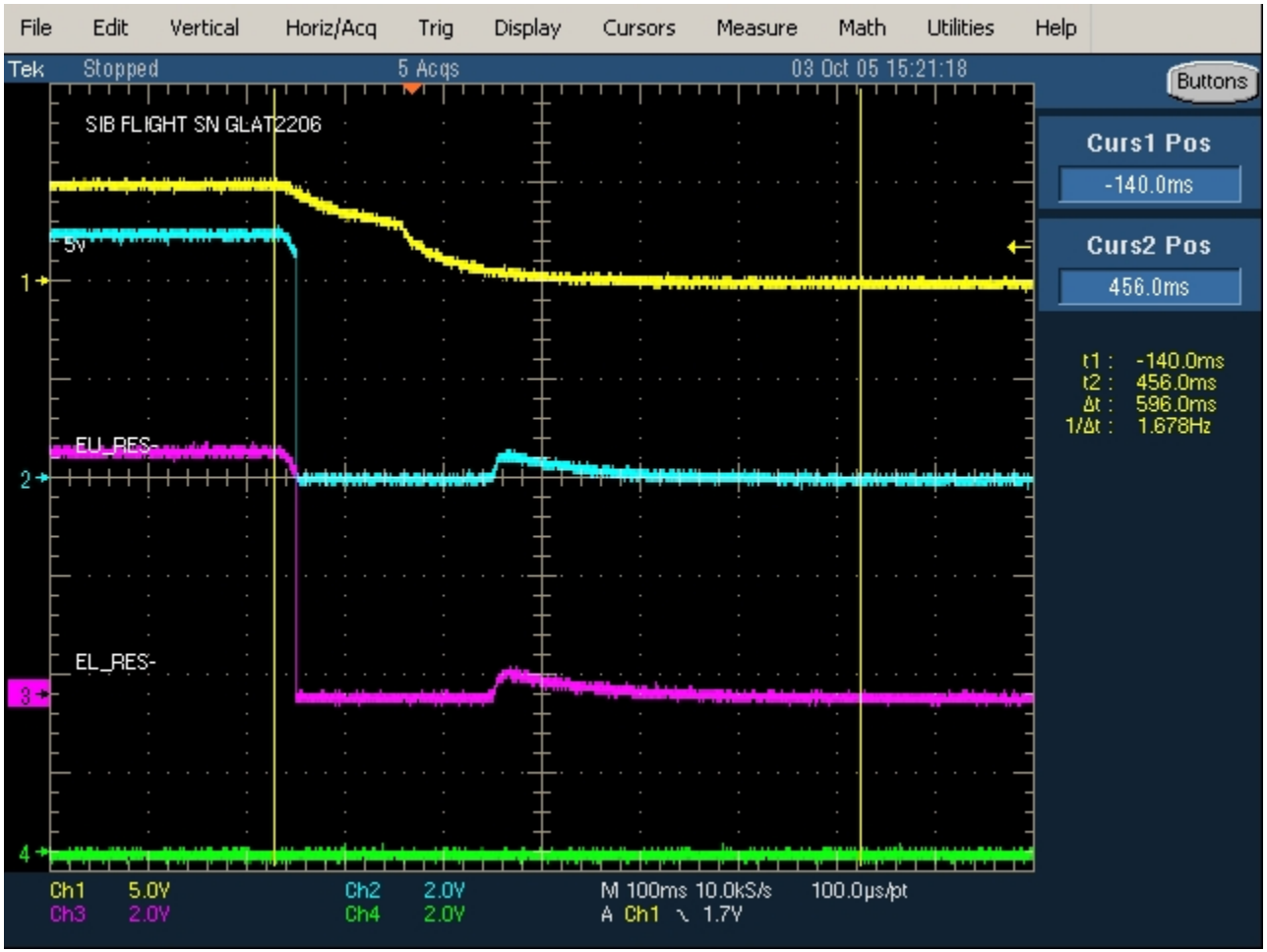
PCI:
PCI:
PCI:
PCI: ----------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: EEPROM WRITE ERROR TEST
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006 .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: M 22800000
22800000 : ffffffff 12345678
22800000 : ffffffff .
PCI:
PCI: M 22000000
22000000 : 00000046 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 46
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: M 22C00000
22c00000 : ffffffff 87654321
22c00000 : ffffffff .
PCI:
PCI: M 22000000
22000000 : 00000086 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 86
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006 .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: END OF WRITE ERROR TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:

```
PCI:
PCI:
PCI: ----------------------------------------------------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: SOFTWARE INTERRUPT TEST
PCI: PAUSE
Press any key to continue...
PCI: M 08000048 C
08000048 : 00000200  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 200
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000000  40
22000004 : 00000040  .
PCI:
PCI: M 08000048 C
08000048 : 00000300  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 300
PCI: PAUSE
Press any key to continue...
PCI: M 08000048 C
08000048 : 00000300  300
08000048 : 00000200  .
PCI:
PCI: M 08000048 C
08000048 : 00000200  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 200
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000040  0
22000004 : 00000000  .
PCI:
PCI: -- END OF REGISTER TEST
PCI: EOS
Script stopped!
PCI:
```

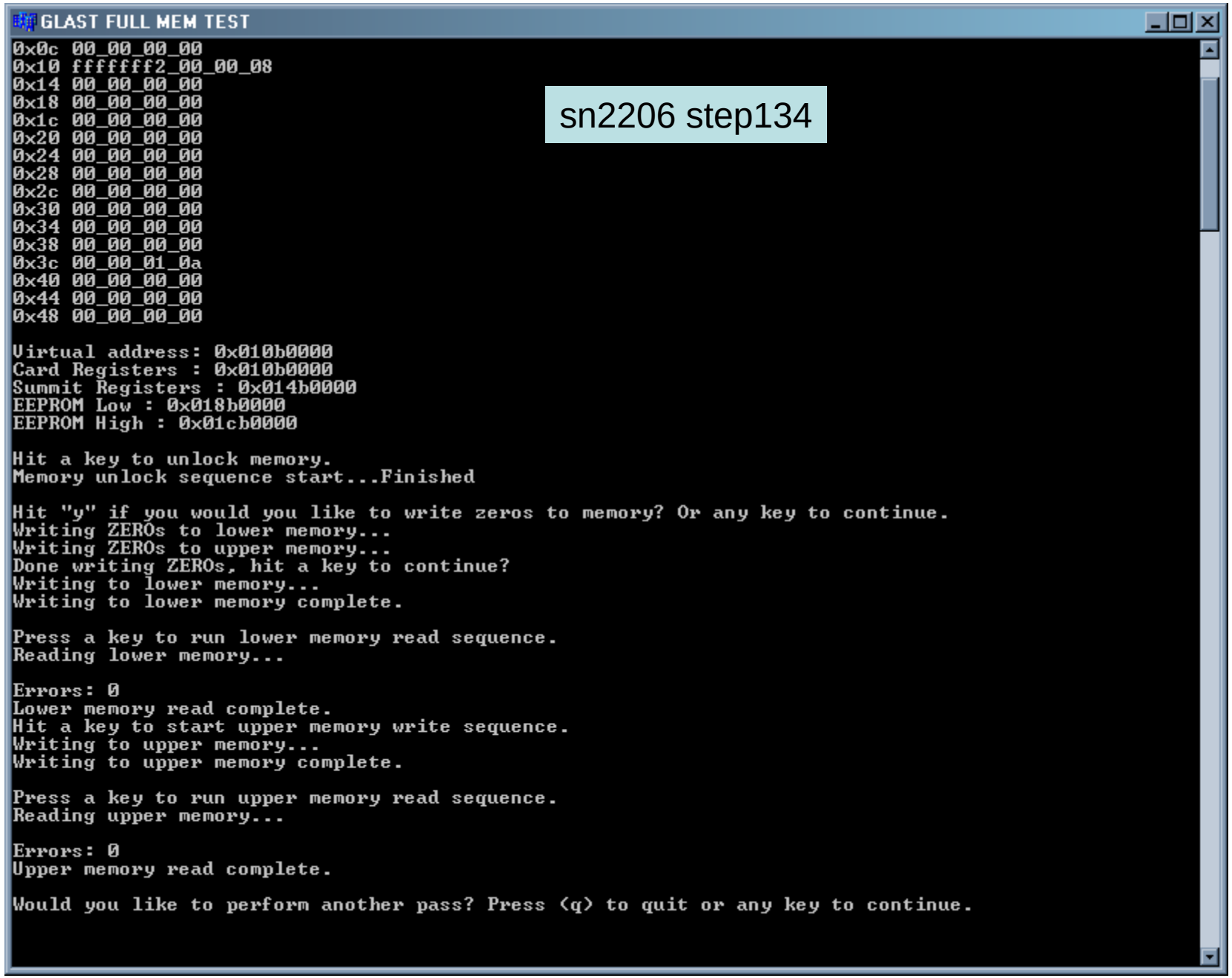
sn2206 step 26d.jpg



SN2206 step 121c.jpg



sn2206 step 121d.jpg


GLAST FULL MEM TEST
0x0c 00_00_00_00
0x10 ffffff2_00_00_08
0x14 00_00_00_00
0x18 00_00_00_00
0x1c 00_00_00_00
0x20 00_00_00_00
0x24 00_00_00_00
0x28 00_00_00_00
0x2c 00_00_00_00
0x30 00_00_00_00
0x34 00_00_00_00
0x38 00_00_00_00
0x3c 00_00_01_0a
0x40 00_00_00_00
0x44 00_00_00_00
0x48 00_00_00_00
Virtual address: 0x010b0000
Card Registers : 0x010b0000
Summit Registers : 0x014b0000
EEPROM Low : 0x018b0000
EEPROM High : 0x01cb0000
Hit a key to unlock memory.
Memory unlock sequence start...Finished
Hit "y" if you would you like to write zeros to memory? Or any key to continue.
Writing ZEROs to lower memory...
Writing ZEROs to upper memory...
Done writing ZEROs, hit a key to continue?
Writing to lower memory...
Writing to lower memory complete.
Press a key to run lower memory read sequence.
Reading lower memory...
Errors: 0
Lower memory read complete.
Hit a key to start upper memory write sequence.
Writing to upper memory...
Writing to upper memory complete.
Press a key to run upper memory read sequence.
Reading upper memory...
Errors: 0
Upper memory read complete.
Would you like to perform another pass? Press (q) to quit or any key to continue.
sn2206 step134

GLAST READ MEM ONLY TEST

sn2206 step139

```
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press (q) to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press (q) to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press (q) to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press (q) to quit or any key to continue.
```

SIB MATE AND DE-MATE LOG SHEET

SIB SN2206 ✓

Note: The SIB card only has the CPCI bus connectors.

Mate or De-Mate	Where	Date	Comment
Mate	SIB Test fixture slot 6	03 OCT 05	OK
De-Mate	"	03 OCT 05	ok
MATE	"	04 OCT 05	OK
De-MATE	"	04 OCT 05	ok

SIB EEPROM WRITE CYCLE LOG SHEET

SIB SN2206

Number of writes	Address	Page or single	Who/when	Running Balance
1	22987264	Single	D. Sellers 03 OCT 05	1
1	22087488	Single		1
12	1 unique address /chip	Single		1
1	All memory	PAGE		2