SIB FLIGHT CARD

TEST RESULTS DOCUMENTATION PACKAGE

SN GLAT2207

20SEPT2005

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(Click on link)

TRAVEL...

SILVER ENGINEERING INC.

HIGH RELIABILITY PRODUCTION TEST

TRAVELER APPROVAL

ENG QA PURCH ASSY DATE 9/15/03

MGR. RELEASE/SHIP TO: DATE

REV	ASSEMBLY NAME	PROCEDURE	ASSY NO.	DRAWING NO.	BOARD & SERIAL NO.	CONTRACT NO.
-	GLAST SIB - Rev 51				ASSY ~~[illegible]~~ LAT-DS-01675-55 SN GLAT 2207	

ITEM	PRODUCTION OPERATION	PARTS VERIFICATION	OPERATOR/ INSPECTOR	DATE START	DATE FINISH	REMARKS	REFERENCE DESIGNATORS
1	Received		DK	9/14/05			
2	Incoming Inspection		JC	9/15/05	9/15/05	U1-44 & U1-43 (almost a solder bridge)	
3	Start procedure SIB Flight Card		DK/JC	9/15/05			
	stopped at step 28					card plugged into wrong slot on Test Fixture	
						inspected slot removed from - good	
						reinstalled Bd into proper slot	
	restart on step 28						
	Stopped Test at step 120		DK/JC		9/15/05	shut down for night	card & test Fixture covered
	start procedure at step 121		DK/JC	9/16/05			
	Stopped Test at step 140						
	waiting to complete for additional Test of memory Test before removing card		Chassis pwr off / Chassis pwr on JC		9/16/05	Tested Good	
4	Removed Card				9/19/05	Tested Good After pwr off for weekend	
5	Prepare to Ship		JC	9/19/05	9/19/05		
6							

TEST PROCEDURE
SIB FLIGHT CARD
LAT-TD-01678 REV 52
12 JULY 2005

Card Assembly Number	LAT-DS-01674 REV 55
Card Serial Number	GLAT 2207
FPGA Label	LAT-DS-03871-52
Test Conductor 1	Dennis Silver
Test Conductor 2	Janet Clifford
Quality Assurance	Janet Clifford
Date of Test	15SEPT 2005

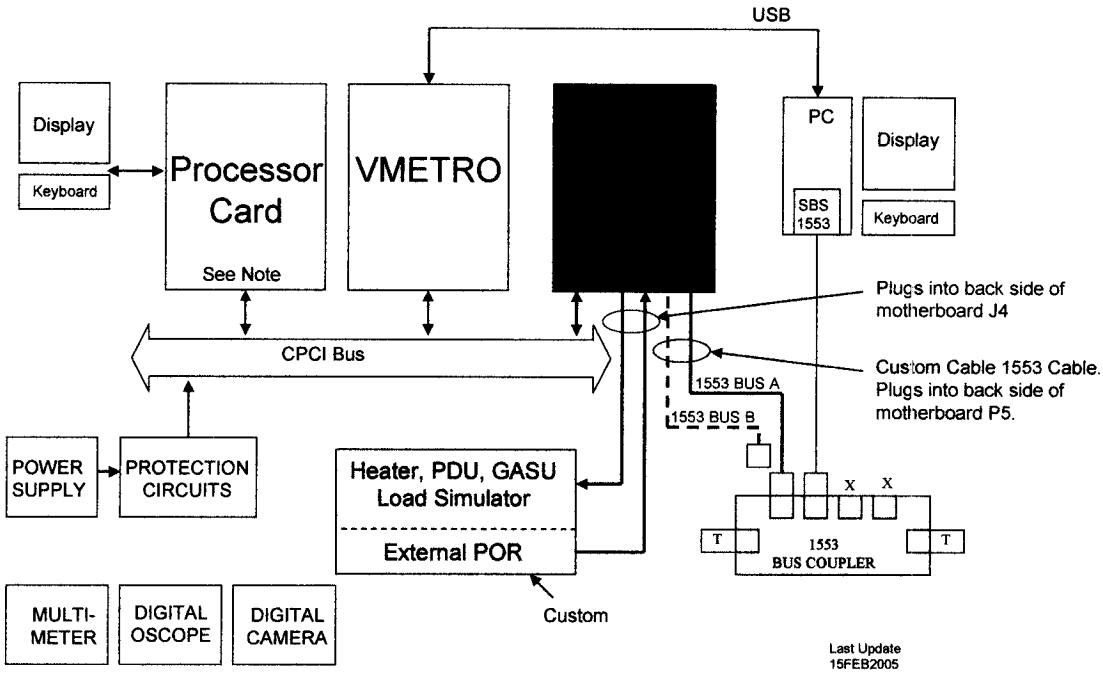
This test procedure shall be used at SEI to test the Flight SIB cards. This procedure assumes the Test Conductors are familiar with the following equipment and software:

VMETRO CPCI emulator
Busview software and scripts
SIB Basics
SBS PCI 1553 card configured as bus controller with PC software
Digital Scope operation
Voltmeter operation

Summary of the tests are as follows:

I. Review and verification of ESD requirements and equipment
II. Continuity testing for card shorts between planes
III. Test fixture power supply test
IV. Verifying voltages on card after power up
V. Verify Actel power switch
VI. Setup and verification of configuration registers
VII. Control/Status Register Test
VIII. EEPROM Unlock Test and Simple EEPROM Write Test
IX. Heater/PDU/GASU test
X. Lower/Upper EEPROM testing:
XI. Lower/Upper EEPROM POR circuit test
XII. SRAM test
XIII. Summit 1553 test, A Bus and B Bus
XIV. 1553 Interrupt test
XV. 1553 SRAM Burst test
XVI. Upper/Lower POR circuit test
XVII. Comprehensive EEPROM Write/Read test

Appendix A Custom 1553 Cable
Appendix B Heater PDU GASU Load Simulator and External POR Generator



Note: Processor Card only installed during Comprehensive EEPROM test.

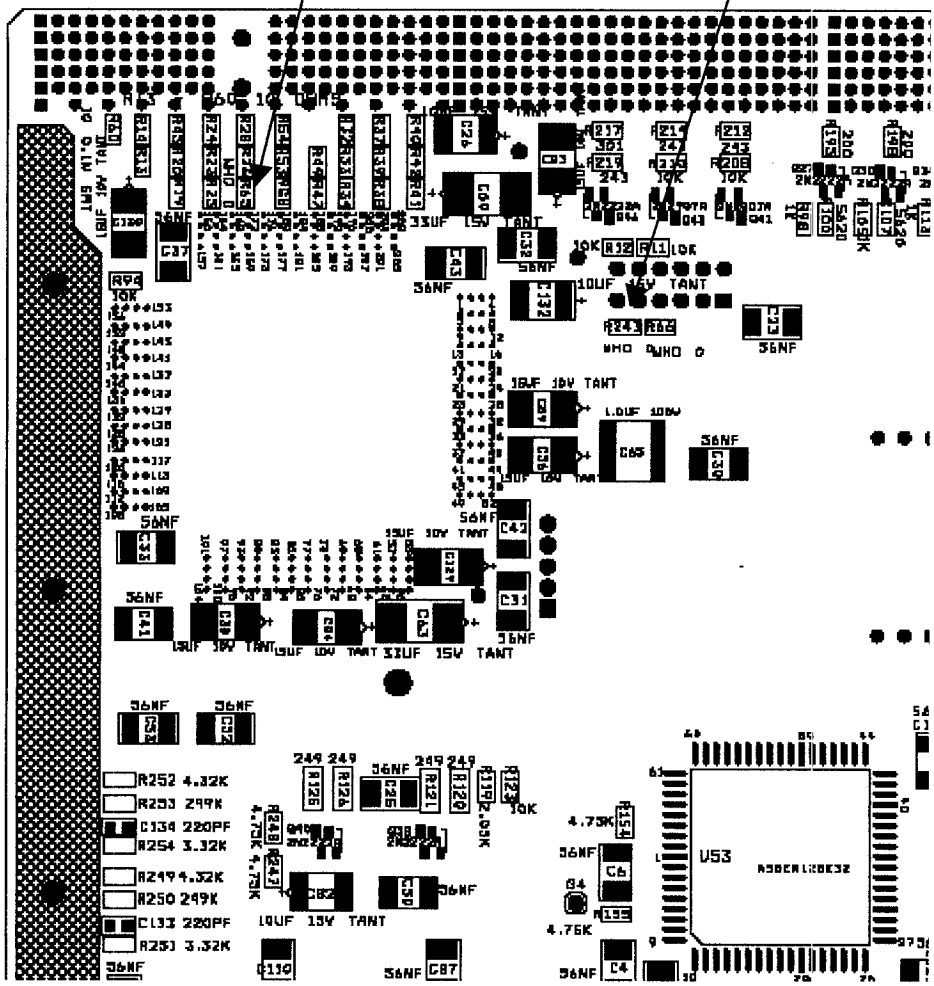
FIGURE 1, Test Configuration

TEST PROCEDURE

Review and verification of ESD requirements and equipment, basic setup

1. Review ESD precautions Yes
2. Test ESD equipment Yes
3. Take pictures of card Yes
4. Visual inspection of card Yes
5. Verify R65 (zero ohm) is **NOT** installed ✓
6. Verify R66 and R243 (zero ohm) are both installed ✓
7. Visual inspection of Capacitor Polarity ✓
8. Visual inspection of SIB CPCI connectors ✓, looked extra hard for alignment looks OK!
9. Visual inspection of Test Fixture connectors ✓

BOTTOM SIDE R65 R66, R243



TC DTA Date 15 Sept 2005 QA JE Date: 15 Sept 2005

Any Problems this page (y/n) Yes If yes, add report **Sh 4 of 30**

SMALL SOLDER TAIL NEAR FPGA PINS U1 43/44

Continuity testing for card shorts between planes

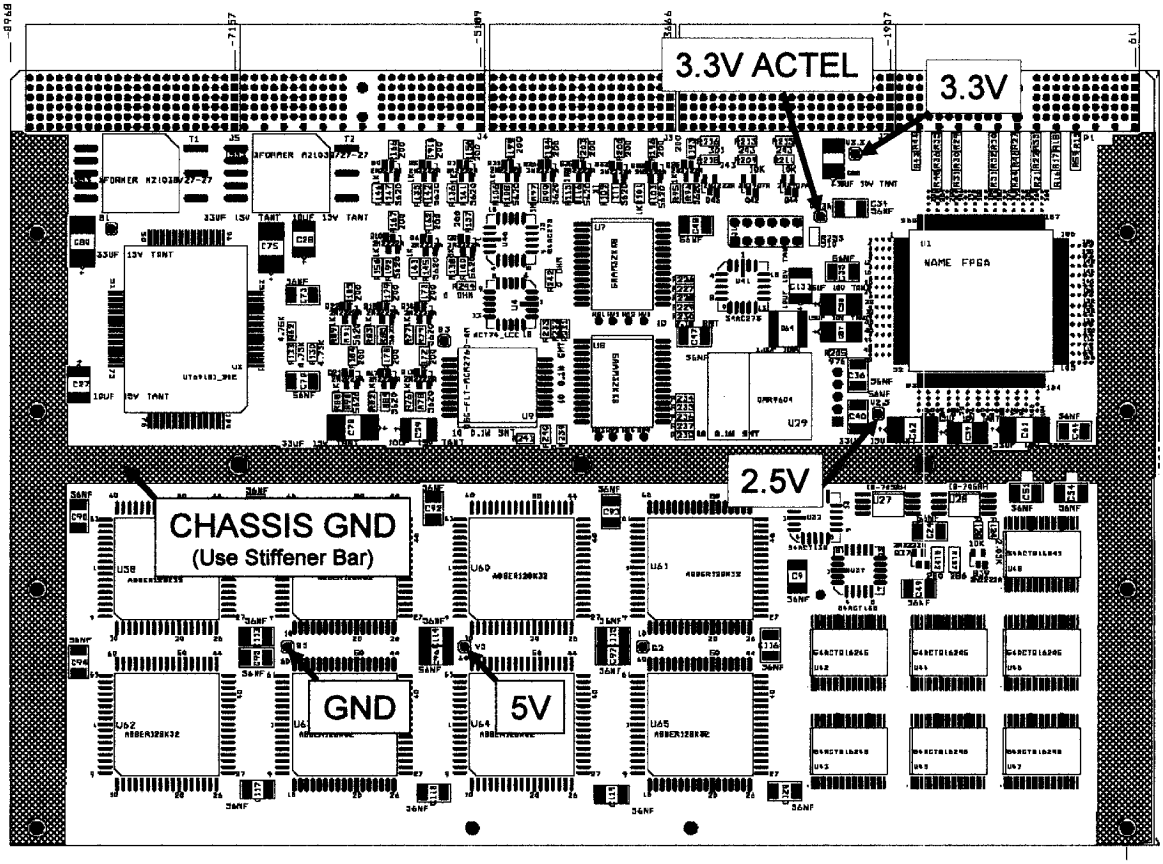
10. Check for shorts by using ohmmeter. Fill in matrix below, use test points as shown in Figure 2.

Red Lead

GND	OPEN				
5V	OPEN	~28K			
3.3V	OPEN	3.8K	25K		
3.3V_ ACTEL	OPEN	510Ω	22K	4.2K	
+2.5	OPEN	239Ω	4.4K	3.9K	750Ω
	CHASSIS GND	GND	5V	3.3V	3.3V_ ACTEL

BLACK lead

11. All open? YES If no, then problem.



TC DTF Date 15 Sept 05 QA JC Date: 9/15/05

Any Problems this page (y/n) N If yes, add report

FIGURE 2, VOLTAGE TEST POINTS

Test fixture power supply test

12. Turn on Test Fixture (no Flight Card Installed) ✓

13. Verify CPCI test fixture power supplies with DVM

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	5.068	✓
3.3V	3.135	3.465	3.327	✓
+12	11.4	+12.6	12.06	✓
-12	-11	-13	-11.45	✓

14. Record 3.3V .001 V @ 50 mOHm mA and 5V .002 V mA @ 50 milliohms currents ✓ 1000mA 2000mA

15. Turn off power supply ✓

Verifying voltages on card after power up

16. Install SIB into test fixture ✓

17. Connect 1553 cable to channel a (channel a can be live, but should not be running) ✓

18. Turn on power supply, ✓

19. Observe card for hot components ✓

20. Verify CPCI test fixture power supplies with DVM

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	5.056	✓
3.3V	3.135	3.465	3.314	✓
+12	11.4	+12.6	12.07	✓
-12	-11	-13	-11.47	✓

.001V @ 50 milliohm .002 V @ 50 milliohm

21. Record +3.3V 1000 mA and +5V 2000 mA currents

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Any Problems this page (y/n) NO If yes, add report

22. Verify SIB <u>on card</u> voltages, reference GND, use test points as shown in Figure 2.

	MIN	MAX	MEASURED	Within limits?
5V	4.75	5.25	5.051	✓
3.3V	3.135	3.465	3.316	✓
3.3V_ ACTEL	3.135	3.465	3.307	✓
+2.5	2.375	2.625	2.560	✓

23. Turn off power supply. ✓

Verify Actel power switch

24. Connect Digital Scope using test points in Figure 2:
- a. Ch 1 2.5V 2v/div
- b. Ch 2 3.3V 2v/div
- c. Ch 3 3.3V_Actel 2v/div
- d. Ch 4 not connected
- e. Trigger Mode Normal, Ch 1 rising, 0.7v
- f. Sweep at 2.5ms/div
- g. ✓

25. Arm scope ✓

26. Turn on power supply —
- a. Observe the following waveform traces ✓
  - i. Ch1 rises from 0V to +2.5V
  - ii. Ch2 rises from 0V to +3.3V ✓
  - iii. Ch3 rises +3.3V after Ch 1 reaches +0.7V
- b. Repeat 5 times ✓, —, —, —, —
- c. Print or photograph waveforms (1 or more) ✓
- d. Label with current time and date SW2207 STEP26D.JPG

TC Dyf Date 15 Sep 05 QA JC Date: 9/15/05
Any Problems this page (y/n) no If yes, add report

Setup and verification of configuration registers

27. Run SIB configuration script (*SIB SLOT6 CONFIG.SCR*) ✓

28. Verify that configuration registers as listed below: ✓

08000000	084411aa	✓
08000004	04000002	✓
08000008	ff000006	✓
0800000c	00000000	✓
08000010	22000008	✓
08000014	00000000	✓
08000018	00000000	✓
0800001c	00000000	✓
08000020	00000000	✓
08000024	00000000	✓
08000028	00000000	✓
0800002c	00000000	✓
08000030	00000000	✓
08000034	00000000	✓
08000038	00000000	✓
0800003c	00000100	✓
08000040	00000000	✓
08000044	00000000	✓
08000048	00000200	✓

Failed due to wrong slot,
Put into correct slot
JC
inspected ~~slot~~ removed
From. good
Re installed Board
into proper slot

Control/Status Register Test

29. Run script *"SIB SLOT6 REG TEST.SCR"* ✓

30. Were all responses correct? ✓

31. What is the current date and time — use SN + step?

32. Highlight screen dump, copy to Word, save as a file name and print, then attach to this test procedure, add date and time to printed file.

SN2207 STEP32.DOC

TC DYS Date 15 Sep 2005 QA JC Date: 9/15/05

Any Problems this page (y/n) NO If yes, add report

EEPROM Unlock Test and Simple EEPROM Write Test

33. Run script 'SIB EEPROM UNLOCK LOWER.scr" ✓

34. Verify status register ✓
   a. PCI: m 22000000
   b. 22000000 : 00000016

35. Write a single memory location in lower EEPROM
   a. ***Note, to minimize rewriting the same EEPROM location incase this test is run more than one time, please select a different memory location each time this test or other special testing has been run in the past. The range for the lower is 22800000 to 22AFFFFE. Also each new memory location written should be more than 8 longword address location different.***
   b. Memory address written = 22987000 with value FEEDDEAD

36. Read memory location written in previous step and verify data matches ✓

37. Verify status register ✓
   a. PCI: m 22000000
   b. 22000000 : 00000016

38. Run script 'SIB EEPROM UNLOCK UPPER.scr" ✓

39. Verify status register ✓
   a. PCI: m 22000000
   b. 22000000 : 00000026

40. Write a single memory location in upper EEPROM
   a. ***Note, to minimize rewriting the same EEPROM location incase this test is run more than one time, please select a different memory location each time this test or other special testing has been run in the past. The range for the lower is 22C00000 to 22EFFFFE. Also each new memory location written should be more than 8 longword address location different.***
   b. Memory address written = 22D87000 with value CAFEBABE

41. Read memory location written in previous step and verify data matches ✓

42. Verify status register
   a. PCI: m 22000000
   b. 22000000 : 00000026 ✓

43. Write Control Register with 00000000 and verify status register ✓
   a. PCI: m 22000004 00000000 ✓
   b. PCI: m 22000000
   c. 22000000 : 00000006 ✓

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Any Problems this page (y/n) NO If yes, add report

Heater/PDU/GASU test

44. Run Script "SIB HEATER_PDU_GASU_TEST.scr"_____
45. Did script pass?_____

SRAM test

46. Run script *"SIB ZERO RAM.scr"*_____
47. Read ram first few locations and verify zero data_____

a. PCI: m 22600000
b. 22600000 : 00000000
c. 22600004 : 00000000
d. 22600008 : 00000000
e. 2260000c : 00000000
f. 22600010 : 00000000
g. 22600014 : 00000000
h. 22600018 : 00000000
i. 2260001c : 00000000
j. 22600020 : 00000000
k. 22600024 : 00000000

48. Run script "*SIB sram walk test.scr*"_____
49. Run script "*SIB sram dumpwalk test.scr*", verify walking 1's, then 0's_____
50. Run script *"SIB ZERO RAM.scr"*_____

a. PCI: m 22600000
b. 22600000 : 00000000
c. 22600004 : 00000000
d. 22600008 : 00000000

Summit 1553 test, A Bus and B Bus

51. Setup Summit for 1553 test

a. Connect up 1553 Bus A Bus Coupler and wiring to Test PC SBS card ✓

b. Run *script "SIB 1553 descriptor block init testds.scr"* ✓

c. Read SRAM_____

i. PCI: m 22608100
ii. 22608100 : 00000000
iii. 22608104 : 00000000
iv. 22608108 : 00000000 ✓
v. 2260810c : 00000000
vi. 22608110 : 00000000
vii. 22608114 : 00000000

d. Read SRAM_____

i. PCI: m 22608000
ii. 22608000 : 00000000
iii. 22608004 : 00000000
iv. 22608008 : 00000001
v. 2260800c : 00000002 ✓
vi. 22608010 : 00000004
vii. 22608014 : 00000008
viii. 22608018 : 00000010
ix. 2260801c : 00000020
x. 22608020 : 00000040
xi. 22608024 : 00000080
xii. 22608028 : 00000100
xiii. 2260802c : 00000200

e. Read SRAM_____

i. PCI: m 22608800
ii. 22608800 : 00000000
iii. 22608804 : 00000000
iv. 22608808 : 0000fffe
v. 2260880c : 0000fffd ✓
vi. 22608810 : 0000fffb
vii. 22608814 : 0000fff7
viii. 22608818 : 0000ffef
ix. 2260881c : 0000ffdf
x. 22608820 : 0000ffbf
xi. 22608824 : 0000ff7f
xii. 22608828 : 0000feff

52. Run SBS Pass 3200 (1553 PC controller software) ✓

53. Connect Remotely = NO ✓

54. Using the pull down menu, >PROJECT >LOAD SETUP > SIB_SETUP.ASU ✓

55. Screen should look like this ✓

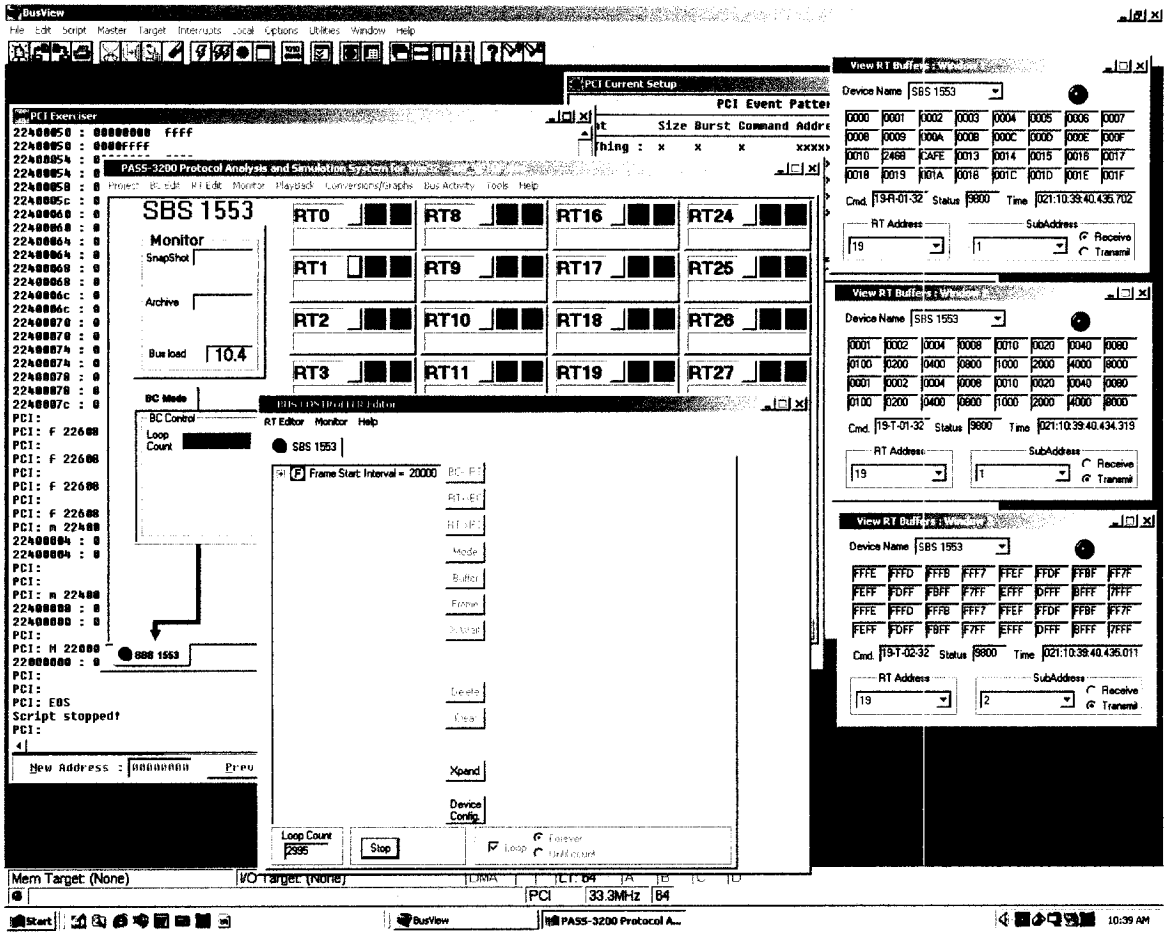


FIGURE 3, SBS 1553 PC SCREEN

56. If SBS software fails to load setup, then it can be configured by running steps (58-61). If SBS software loads ok, you can skip steps58-61.

57. Can you skip steps 58-61? ✓

58. Select BC Edit_____

59. Select RT to BC_____

a. Select RT Address 19
b. Select RT Sub Address 1
c. Select Word Count 32

SKIP
correct screens opened already

60. Select RT to BC_____

a. Select RT Address 19
b. Select RT Sub Address 2

TC DLA Date 15 Sept 05 QA JC Date: 9/15/05
Any Problems this page (y/n) no If yes, add report

c. Select Word Count 32

61. Select BC to RT_____
   a. Select RT Address 19
   b. Select RT Sub Address 1
   c. Select Word Count 32
   d. Select Date Buffer 1
   e. Type data FEED in location 1
   f. Type data DEAD in location 2
   g. Type data BEEF in location 3
   h. Type data BABE in location 4
   i. Type data FACE in location 5
   j. Type data CAFE in location 6
   k. Type data 5A5A in location 7
   l. Type data A5A5 in location 8
   m. Type data F0F0 in location 9
   n. Type data 0F0F in location 10
   o. Select BR to end data buffer 1 edit
   p. Select BUS A
   q. Select Continue on Error
   r. Select Loop Forever

skip

62. Select RUN___✓___
63. Verify Green Monitor Lamp at top of BC Editor Screen___✓___
64. Select Main SBS1553 Pass 3200 screen. _____✓
   a. Verify that RT 19 is illuminated green
   b. Verify that the Loop Count Indicator is incrementing
65. Select Bus Activity___✓___

66. Select Percent Display___✓___
   a. Verify that RT 19 is receiving about 33% of the time ✓
   b. Verify that RT 19 is transmitting about 67% of the time ✓
67. Select OK___✓___
68. Select Bus Activity___✓___
69. Select Bus Count Analysis___✓___
   a. Verify that RT 19 CMD Count is incrementing with NO Errors ✓
70. Select OK___✓___
71. Select Monitor___✓___
72. Select RT Viewers___✓___ (three should be already be in view)
73. Select Sub Address 1, Receive___✓___
   a. Verify monitor lamp is illuminated green and status=9800

Verify 32 words of data that matches data buffer 1

74. Select Sub Address 1, Transmit___✓___
   a. Verify monitor lamp is illuminated green and status=9800
   b. Verify 32 words of walking ones data ✓

75. Select Sub Address 2, Transmit ✓
   a. Verify monitor lamp is illuminated green and status=9800 ✓
   b. Verify 32 words of walking zeros data from FFFE to 7FFF ✓

76. Select Bus View and verify data ✓
   a. PCI: m 22608100
   b. 22608100 : 00000200 (actual data may vary)
   c. 22608104 : 0000862f (actual data may vary)
   d. 22608108 : 0000feed
   e. 2260810c : 0000dead
   f. 22608110 : 0000beef
   g. 22608114 : 0000babe
   h. 22608118 : 0000face
   i. 2260811c : 0000cafe
   j. 22608120 : 00005a5a ✓
   k. 22608124 : 0000a5a5
   l. 22608128 : 0000f0f0
   m. 2260812c : 00000001
   n. 22608130 : 00000002
   o. 22608134 : 00000003

77. At location 22608138 write 7777, hit ENTER, Press P and verify that it returns to the value 4 ✓
   PCI : m 22608138
   a. 22608138 : 00000004 7777
   b. 22608138 : 00007777 (note, sometimes the data is overwritten to value 4)
   c. 22608134 : 00000003 ✓
   d. 22608138 : 00000004
   e.

78. Select BC Edit then select STOP ✓

79. Remove 1553 Bus cable from A ✓

80. Summit Reset, ✓
   a. PCI: m 22000004
   b. 22000004 : 00000000 80 ✓
   c. 22000004 : 00000080 0

81. Run script *"SIB ZERO RAM.scr"* ✓

   a. Connect up 1553 Bus **B** Bus Coupler and wiring to Test PC SBS card ✓

   b. Run *script "SIB 1553 descriptor block init testds.scr"* ✓

c. Read SRAM ✓
   i. PCI: m 22608100
   ii. 22608100 : 00000000
   iii. 22608104 : 00000000
   iv. 22608108 : 00000000
   v. 2260810c : 00000000 ✓
   vi. 22608110 : 00000000
   vii. 22608114 : 00000000

d. Read SRAM ✓
   i. PCI: m 22608000
   ii. 22608000 : 00000000
   iii. 22608004 : 00000000
   iv. 22608008 : 00000001
   v. 2260800c : 00000002 ✓
   vi. 22608010 : 00000004
   vii. 22608014 : 00000008
   viii. 22608018 : 00000010
   ix. 2260801c : 00000020
   x. 22608020 : 00000040
   xi. 22608024 : 00000080
   xii. 22608028 : 00000100
   xiii. 2260802c : 00000200

e. Read SRAM
   i. PCI: m 22608800
   ii. 22608800 : 00000000
   iii. 22608804 : 00000000
   iv. 22608808 : 0000fffe
   v. 2260880c : 0000fffd ✓
   vi. 22608810 : 0000fffb
   vii. 22608814 : 0000fff7
   viii. 22608818 : 0000ffef
   ix. 2260881c : 0000ffdf
   x. 22608820 : 0000ffbf
   xi. 22608824 : 0000ff7f
   xii. 22608828 : 0000feff

82. Select BC Edit then select RUN ✓

83. Verify Green Monitor Lamp at top of BC Editor Screen ✓
84. Select Main SBS1553 Pass 3200 screen. ✓
   a. Verify that RT 19 is illuminated green
   b. Verify that the Loop Count Indicator is incrementing ✓
85. Select Bus Activity ✓

86. Select Percent Display ✓
  a. Verify that RT 19 is receiving about 33% of the time ✓
  b. Verify that RT 19 is transmitting about 67% of the time ✓
87. Select OK ✓
88. Select Bus Activity ✓
89. Select Bus Count Analysis ✓
  a. Verify that RT 19 CMD Count is incrementing with NO Errors
90. Select OK ✓
91. Select Monitor ✓
92. Select RT Viewers ✓ ALL Ready ON
93. Select New RT Viewer ✓
94. Select RT Address 19 ✓
95. Select Sub Address 1, Receive ✓
  a. Verify monitor lamp is illuminated green and status=9800 ✓
  b. Verify 32 words of data that matches data buffer 1
96. Select Sub Address 1, Transmit ✓
  a. Verify monitor lamp is illuminated green and status=9800 ✓
  b. Verify 32 words of walking ones data ✓
97. Select Sub Address 2, Transmit ✓
  a. Verify monitor lamp is illuminated green and status=9800 ✓
  b. Verify 32 words of walking zeros data from FFFE to 7FFF ✓
98. Select Bus View and verify data ✓
  a. PCI: m 22608100
  b. 22608100 : 00000200 (actual data may vary)
  c. 22608104 : 0000862f (actual data may vary)
  d. 22608108 : 0000feed
  e. 2260810c : 0000dead
  f. 22608110 : 0000beef
  g. 22608114 : 0000babe
  h. 22608118 : 0000face
  i. 2260811c : 0000cafe
  j. 22608120 : 00005a5a
  k. 22608124 : 0000a5a5
  l. 22608128 : 0000f0f0
  m. 2260812c : 00000001
  n. 22608130 : 00000002
  o. 22608134 : 00000003
99. At location 22608138 write 7777, hit ENTER, Press P and verify that it returns to the value 4 ✓
  a. PCI : m 22608138
  b. 22608138 : 00000004 7777
  c. 22608138 : 00007777 (note, sometimes the data is overwritten to value 4)
  d. 22608134 : 00000003
  e. 22608138 : 00000004 ✓

1553 Message Interrupt test

100. Note, 1553 should still be running from previous test ✓

101. Select BC Edit then select STOP ✓

102. Clear possible interrupt in configuration register by writing 300. Read 08000048 multiple time should always be 200 ✓

a. PCI: M 08000048 C
b. 08000048 : 00000300 300
c. 08000048 : 00000200
d. 08000048 : 00000200
e. 08000048 : 00000200
f. 08000048 : 00000200

103. Select BC Edit then select Run ✓

104. Clear possible interrupt in configuration register by writing 300 (several times). Read 02000048 multiple time should always revert back 300 ✓

a. 08000048 : 00000300 300
b. 08000048 : 00000300 300
c. 08000048 : 00000300 300
d. 08000048 : 00000200 Note, sometimes afterwriting 300, it will still be 200, but the next read will be 300
e. 08000048 : 00000300
f. 08000048 : 00000300 300
g. 08000048 : 00000300
h. 08000048 : 00000300

1553 You Fail Interrupt test

105. Select BC Edit then select STOP ✓

106. Clear possible interrupt in configuration register by writing 300. Read 08000048 multiple time should always be 200 ✓

a. PCI: M 08000048 C
b. 08000048 : 00000300 300
c. 08000048 : 00000200
d. 08000048 : 00000200
e. 08000048 : 00000200
f. 08000048 : 00000200

107. Interrupt test, Turn on VMETRO Trace ✓

108. Force YF_INT (You Fail) ✓
a. PCI: M 22400010
b. 22400010 : 00000400
c. 22400010 : 00000000
d. 22400010 : 00000000
e. 22400010 : 00000000 1000
f. 22400010 : 00001000

109. Verify Interrupt was received ✓
a. PCI: M 08000048 C
b. 08000048 : 00000300
c. 08000048 : 00000300
d. 08000048 : 00000300 300
e. 08000048 : 00000200
f. 08000048 : 00000200
g. 08000048 : 00000200
h. 08000048 : 00000200
i. 08000048 : 00000200

110. Halt Trace and Show Trace, verify Interrupt went active, then inactive ✓

111. Select BC Edit then select Run ✓

1553 SRAM BURST TEST

112. Verify 1553 bus is running ok. ✓

113. Run *Script SIB SRAM BURST TEST.scr* ✓

114. Verify 1553 bus is running ok. ✓

115. Run >Script >RUN LOOP 1000 ✓

116. Verify 1553 bus is running ok during loop. ✓
(Reference Figure 3

All Good.

Lower/Upper EEPROM POR Circuit Test

117. Using voltmeter, measure voltages at R249 and R252 probe points. Reference Figure 4.

a. Voltage at R249 1,461
b. Voltage at R252 1,466
c. Range should be 1.40V to 1.49V ✓

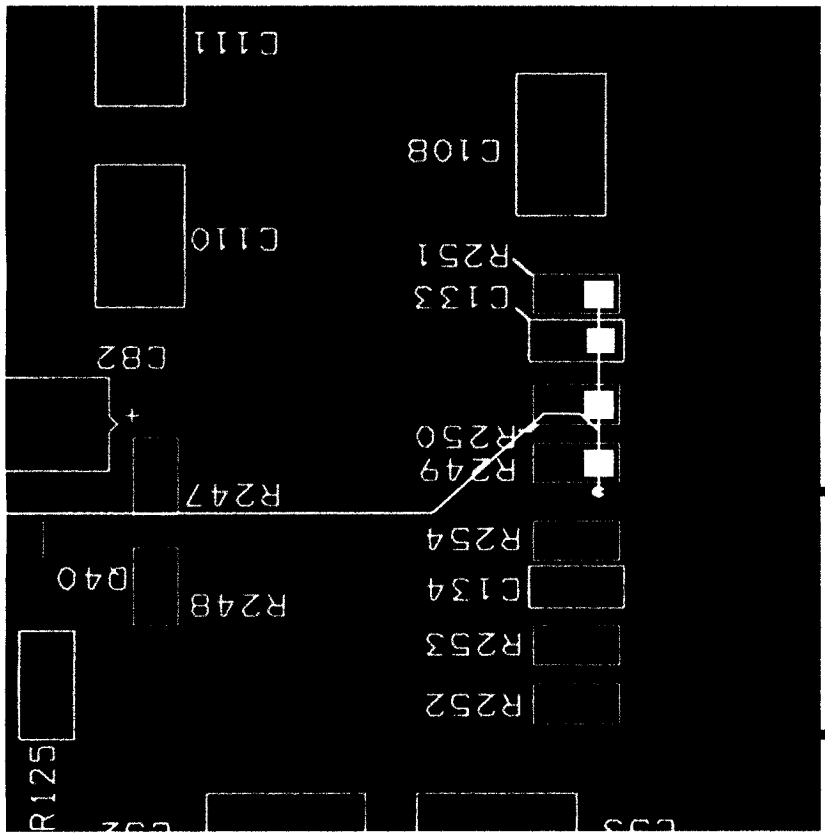


FIGURE 4, POR Probe Points (as viewed from bottom side of CCA in test fixture)

118. Run Script *"SIB POR Mem test.scr"* (*read step a. first*) Must Run

a. Note this step does not need to be done if data already exist in memory. Run Script *"SIB POR Mem dump test.scr"* and if data counts up do not run script *"SIB POR Mem test.scr"* ✓

119. Verify POR connects to all memory in Upper Bank

a. Run Script "*SIB POR Mem dump test.scr*" ✓
b. Data should increment? ✓
c. Connect or Hold special Test Lead #1 with built in 3.3K resistor to Gnd at R249 Probe Point ✓
d. Run Script "*SIB POR Mem dump test.scr*" ✓
e. Data in address range 22C00000 to 22EFFFC should be all F's and only Lower Address range (22800000 to 22AFFFFC) should increment ✓
f. Remove Probe ✓

120. Verify POR connects to all memory in Lower Bank

a. Run Script "*SIB POR Mem dump test.scr*" ✓
b. Data should increment? ✓
c. Connect or Hold special Test Lead #1 with built in 3.3K resistor to Gnd at R252 Probe Point ✓
d. Run Script "*SIB POR Mem dump test.scr*" ✓
e. Data in address range 22800000 to 22AFFFC should be all F's and only Upper Address range (22C00000 to 22EFFFFC) should increment ✓
f. Remove Probe ✓
g. Power off test chassis

TC DYL Date 15 Sept 2005 QA JC Date: 9/15/05
Any Problems this page (y/n) NO If yes, add report

121. Verify POR works during powerup/power down. Reference probe points in Figure 5.

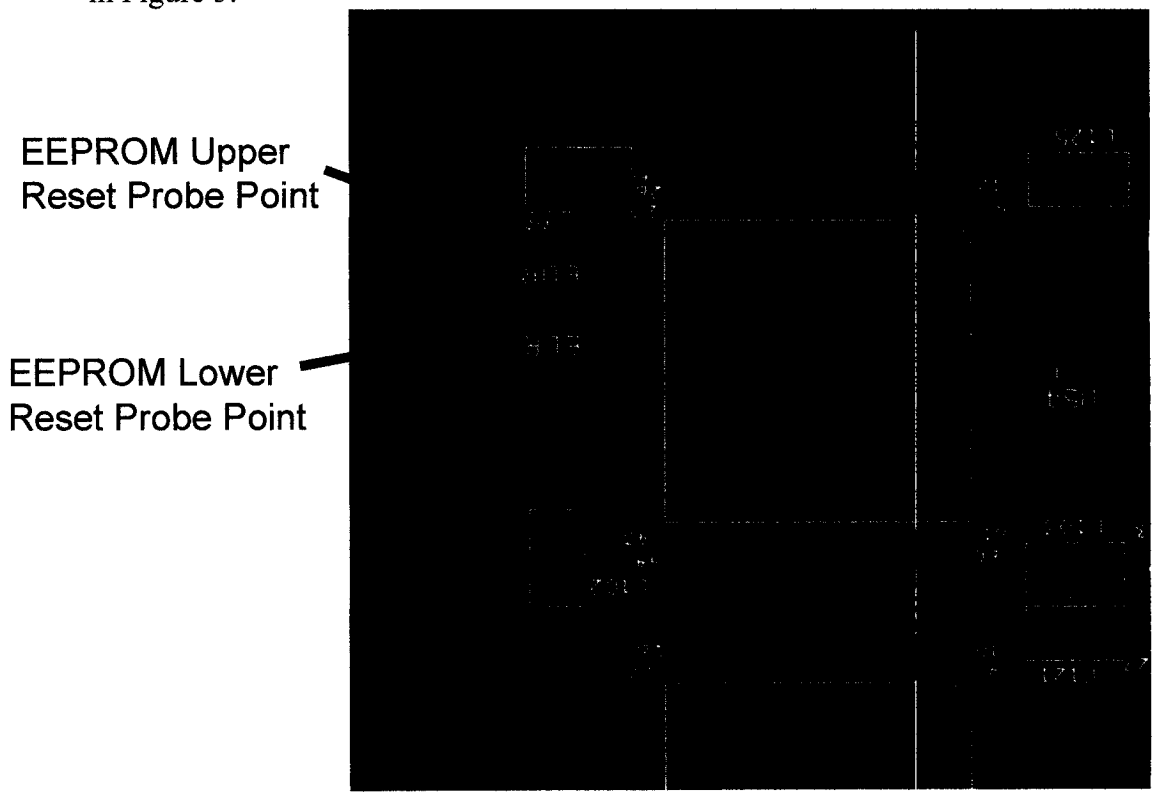


FIGURE 5, Upper and Lower EEPROM Reset Probe Points (as viewed from back side of CCA while in test fixture)

a. Adjust scope
   i. ch 1 = 5v/div, 2, & 3 = 2v/div, ✓ (label scope +5v, EU_RES-, EL_RES-)
   ii. 40ms sweep ✓
   iii. Trigger on Channel 1 Rising ✓

b. Connect Scope leads
   i. Ch 1 to +5V on test chassis
   ii. Ch 2 to EEPROM Upper Reset Probe Point
   iii. Ch 3 to EEPROM Lower Reset Probe Point

c. Adjust scope:
   i. Cycle power on and verify EEPROM Upper and Lower Reset POR lags +5v by appx 180-220ms ✓
   ii. Repeat 5 times ✓, ✓, ✓, ✓, ✓
   iii. Photograph or print waveform (just 1) ✓
   iv. Label Photo/Print with current time and date SNZZ07 SctP12IC4.JPG

TC DLS Date 16 Sept 05 QA JC Date: 9/16/05
Any Problems this page (y/n) NO If yes, add report

d. Adjust scope: 2v, trig ch 1 falling normal, H~~40~~100ms, ✓
   i. Cycle power off and verify POR goes low while +5 decays ✓
   ii. Repeat 5 times ✓, ✓, ✓, ✓, ✓
   iii. Photograph or print waveform (just 1) ✓
   iv. Label Photo/Print with current time and date ✓
e. Turn off test fixture

SN27075TVP121D4.JPG

TC DLS Date 16 Sept 2005 QA JC Date: 9/14/05
Any Problems this page (y/n) NO If yes, add report

Comprehensive EEPROM Write/Read test

122. Install Processor card into test chassis and boot system. ✓

123. Turn off virus protection software ✓

124. Make sure no screen savers are on ✓

125. Unplug network cable ✓

126. Open power point and minimize (to be used for screen capture) ✓

127. Run GLAST FULL MEM TEST, reference Figure 6

FIGURE 6, GLAST Full Memory Test screen capture.

128. Press any key to unlock memory ✓

129. Hit "y" to write zeros in memory (this takes 4 minutes) ✓

130. Press any key to run lower memory write (this takes 2 minutes) ✓

131. Press any key to run lower memory read. Any errors? ✓ NO

132. Press any key to run upper memory write (this takes 2 minutes) ✓ Yes

133. Press any key to run upper memory read. Any errors? NO

134. Save screen capture to power point file and name file with the current date and time SN220755EP134.PPT

TC DH Date 16 Sept 2005 QA JC Date: 9/14/05

Any Problems this page (y/n) NO If yes, add report

135. Press q to quit ✓

136. Run GLAST READ MEM ONLY TEST, reference Figure 7

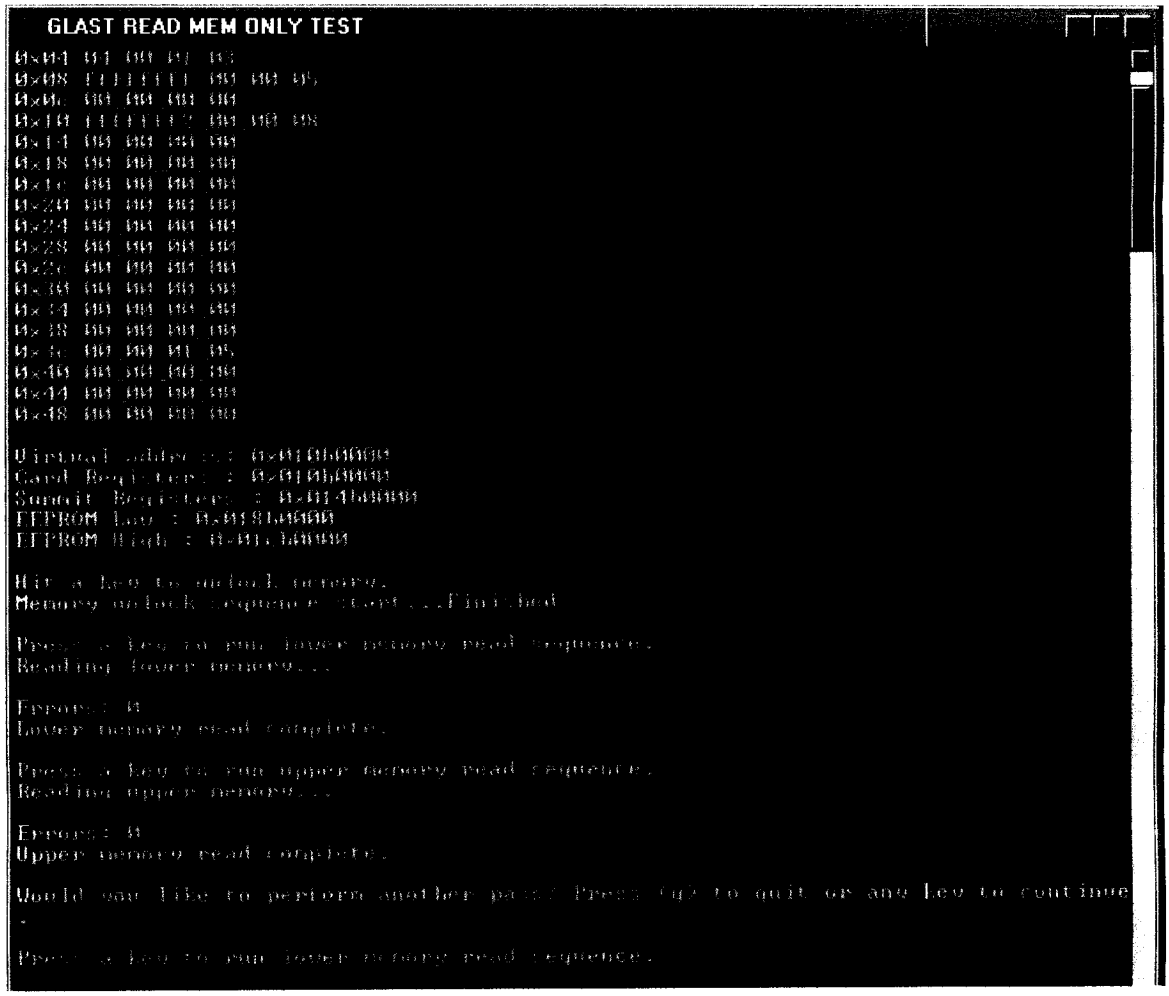


FIGURE 7, GLAST READ MEM ONLY TEST screen capture

137. Hit any key to run read of upper and lower eeprom 10 times ✓

138. Any Errors reported? NO

139. Capture screen and add to power point file. ✓

140. Close program ✓ RAN EXTRA Read Only Test, OK ✓

141. Remove card, inspect cPCI connectors on text fixture and SIB ✓

142. Take post test pictures of card —

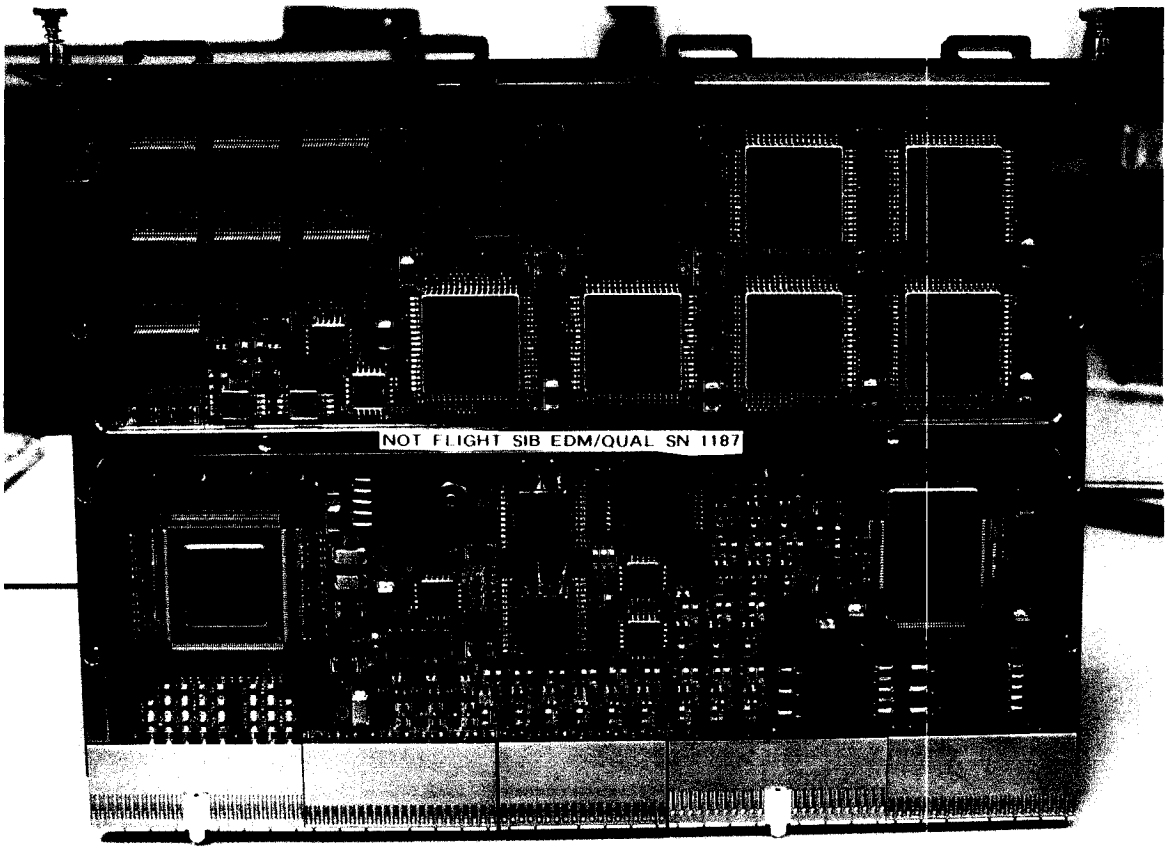
143. Attach printouts, photographs, and pertinent information to signed test report.

144. TEST COMPLETE

Thursday
Monday Sept 19 2005

TC DPL Date 19 Sept 2005 QA JC Date: 9/19/05

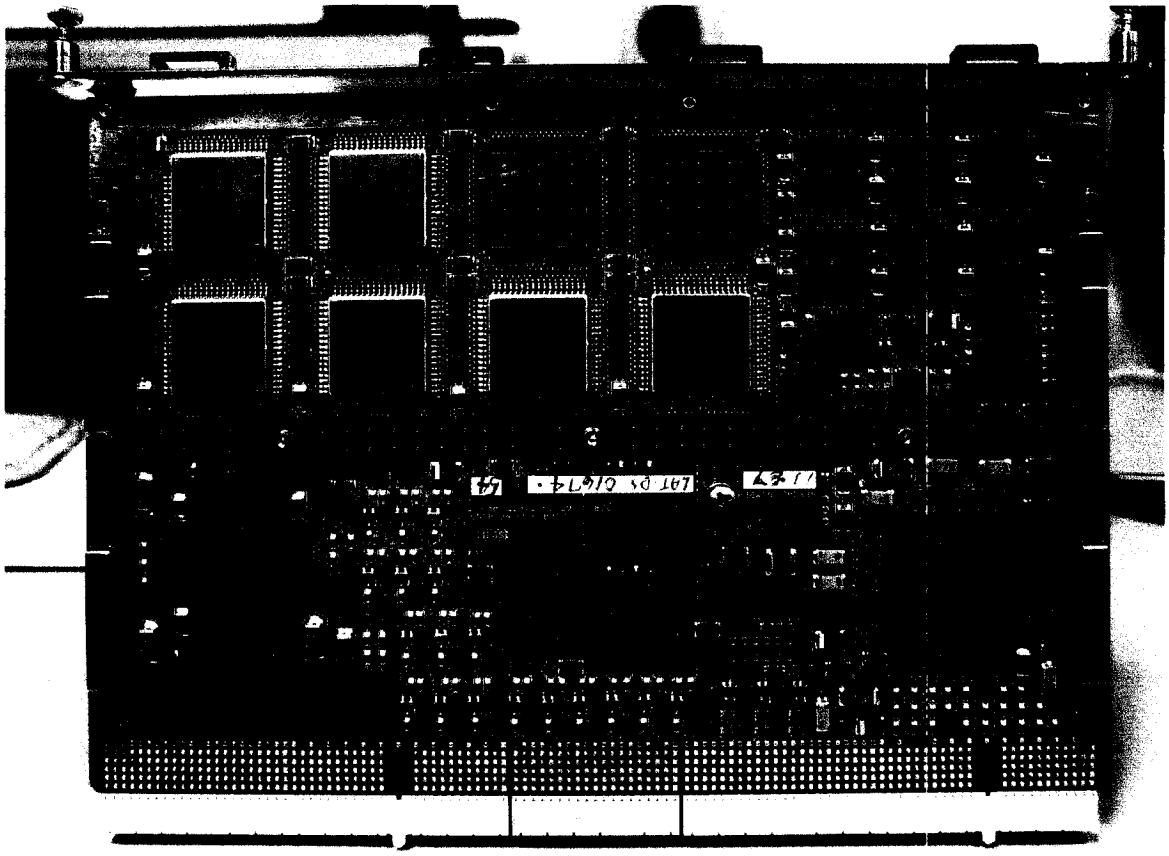
Any Problems this page (y/n) NO If yes, add report



GLAST SIB LAT-DS-01675 REV 51 TOP SIDE

NA

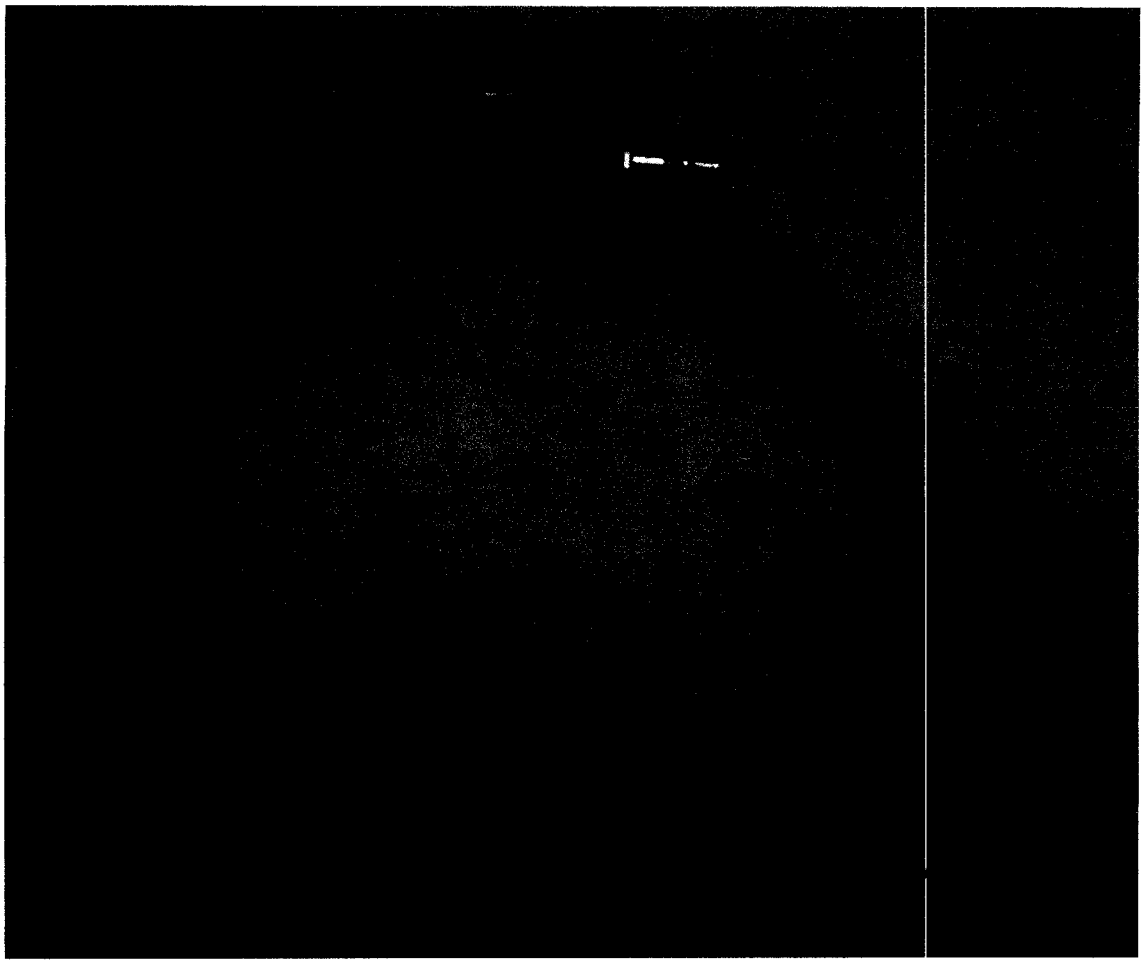
TC_____Date_____ QA_____Date:_____
Any Problems this page (y/n)_____ If yes, add report



GLAST SIB LAT-DS-01675 REV 51 BOTTOM SIDE

NA

TC_____Date_____ QA_____Date:_____
Any Problems this page (y/n)_____ If yes, add report



All I/O for the SIB is via the backplane interface. This custom cable connects to the CPCI motherboard P5 and brings out 1553 Bus A and Bus B.

Figure 1 and 2 are pictures of the Heater PDU GASU Load Simulator and External POR generator. A simplified schematic is shown in Figure 3. This simulator plugs into the CPCI motherboard J4 connect in the slot with the SIB under test.

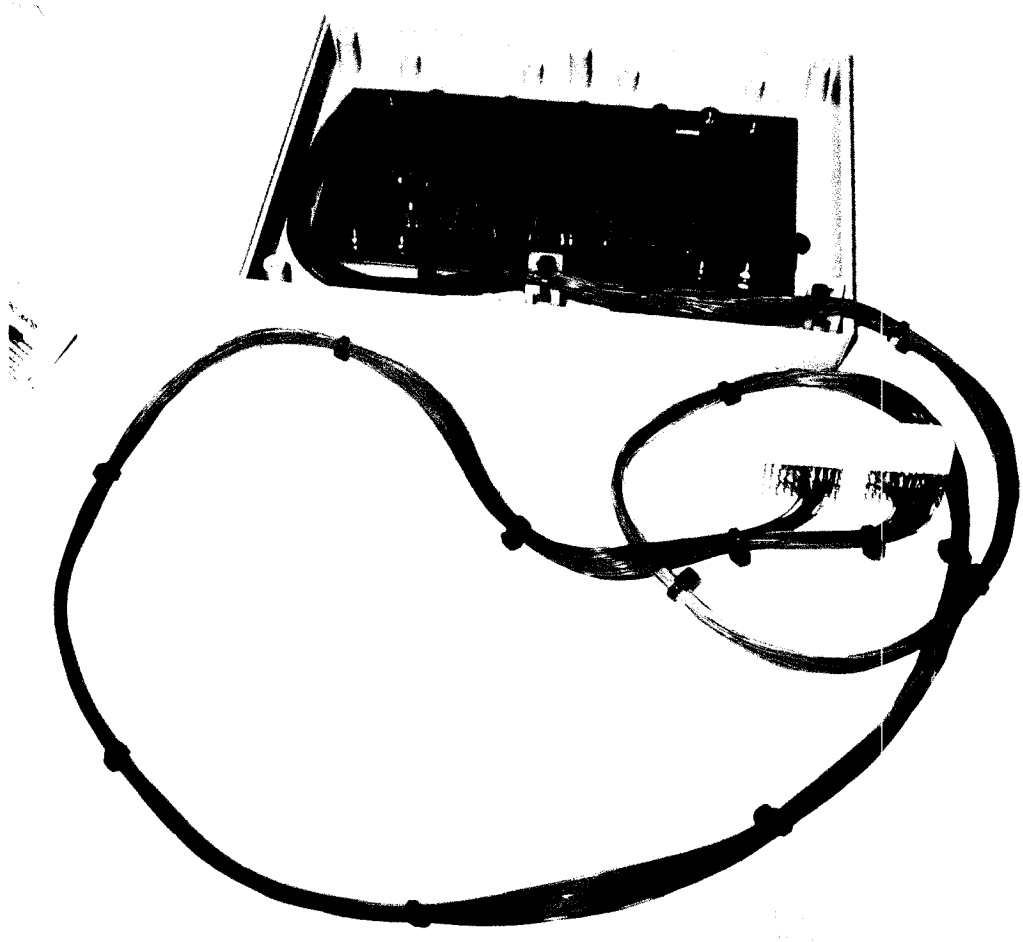


Figure 1 Photo of Heater PDU GASU Load Simulator and External POR

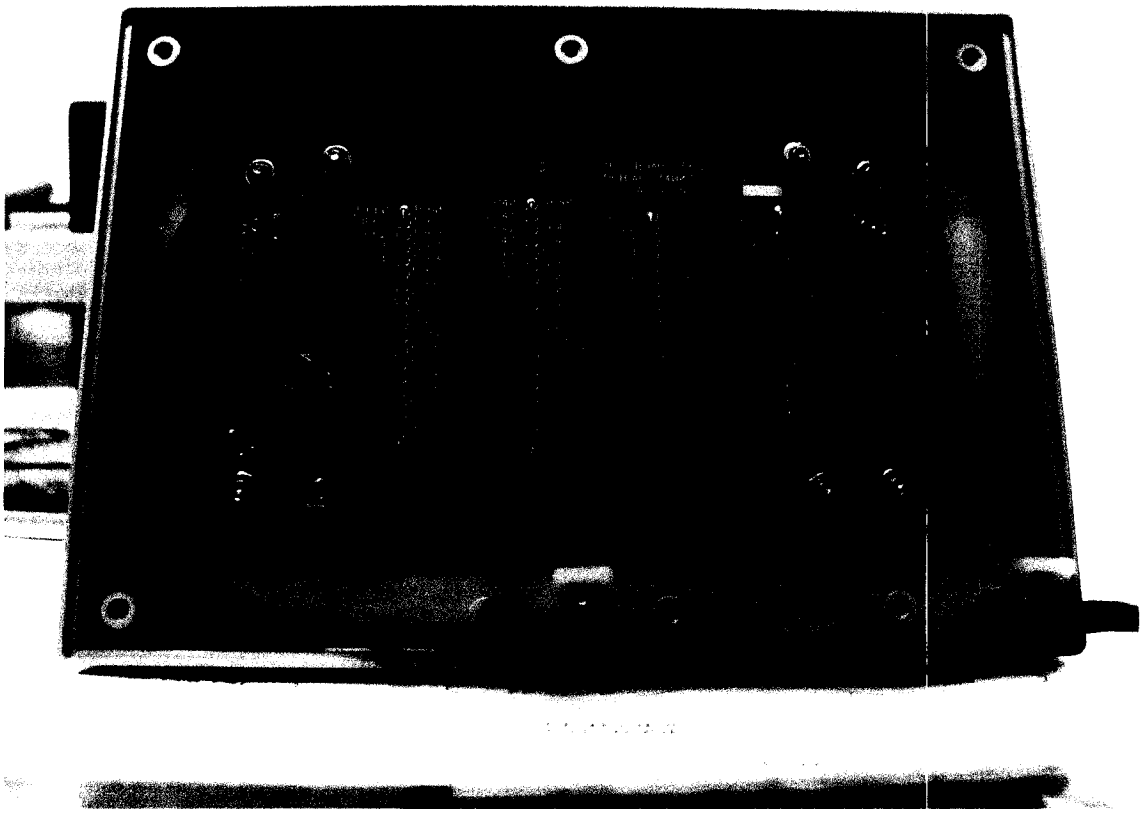


Figure 2 Close Up Photo of Heater PDU GASU Load Simulator and External POR

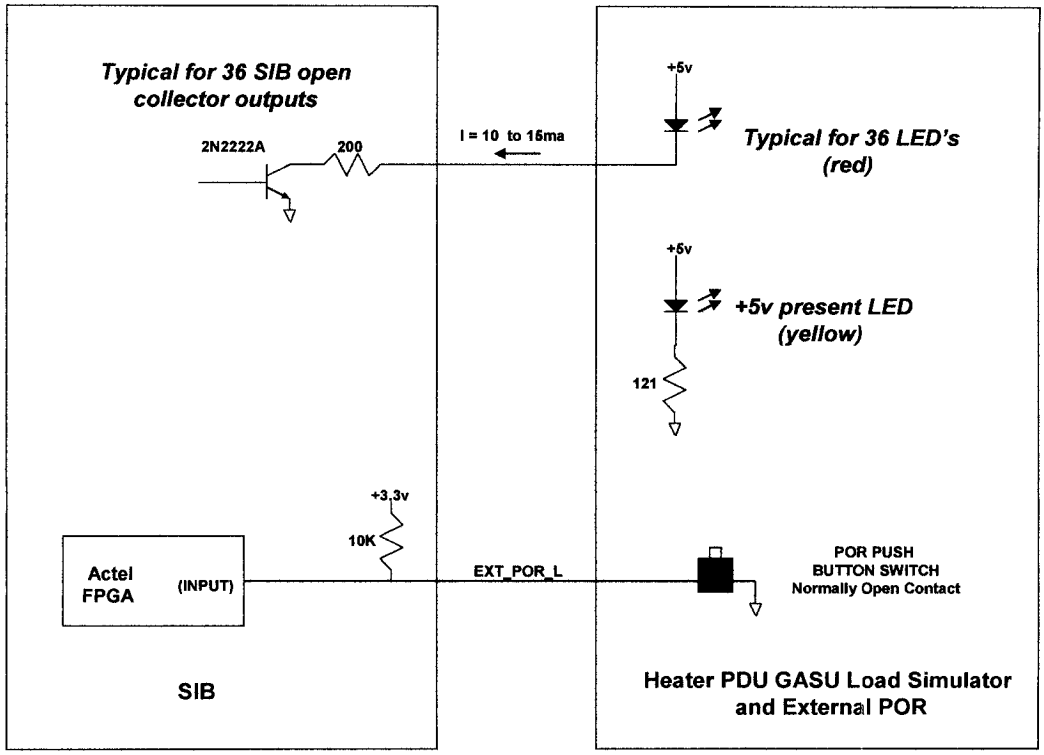


Figure 3, Simplified schematics of Heater PDU GASU Load Simulator and External POR

SIB FLIGHT SN GLAST2207

LAT-DS-01674
REV55

15 SEPT 2005

1. Received Package 14 SEPT 2005
   (2 CARDS
2. SHOCK SENSORS OK FOR BOTH
3. BEGAN VISUAL INSPECTION ON 15 SEPT 2005 of TRAVELER
4. FOUND ONE SOLDER JOINT WITH LONG TALE THAT SHOULD BE FIXED, TOOK PICTURES IMG_5200.JPG & 5201
5. THE REST OF CARD LOOKS GREAT!
6. We took special look at CPCI connectors from a memo from MARK FREYTAG email 9/14/2005
   CPCI connectors look OK!
7. Procedures 1-11 OK
8. Procedure 12-27, OK
9. Sept 28 Failed, card in wrong slot!
10. Removed CARD Inspected slot, OK
11. Plugged into correct slot
12. Started at step 28
13. Steps 28-120 ALL GOOD

Skip to SM 7

MATE + DeMATE LOG SN 2207

1. MATE 15 Sept 05
2. Demate 15 Sept 05
3. MATE 15 Sept 05
4. DeMATE SEPT 19th 05

MATE & Demate LOG SN 2208

1. MATE 19 Sept
2. Demate 19 SEPT

SN2207

(14) 7:30Pm Shut down & covered CARD

(15) 16 Sept 2005 9:09 Am

(16) Uncovered & Turn on PC & Scope

(17) Did ESD log

(18) START Test procedure @ Step 121

(19) 121 - 140 ALL GOOD

(20) Turn off power at 9:53 Am

(21) Turn power on 1:45 Pm

RAW EEPROM Read only TEST

PASSED !! This was extra.

(22) Turned off PWR to Chassis (Appx 2:30 P

(23) Monday, Sept 19 2005, 10:00 Am

Power on Test Chassis

(24) DID EEPROM READ ONLY TEST

PASS OK! Memory ok over weekend!

(25) DID ESD TEST, Removed CARD, TOOK PICS

(26) BAGGED + Boxed, Shipped 19 Sept 2005

SN GLAT2207

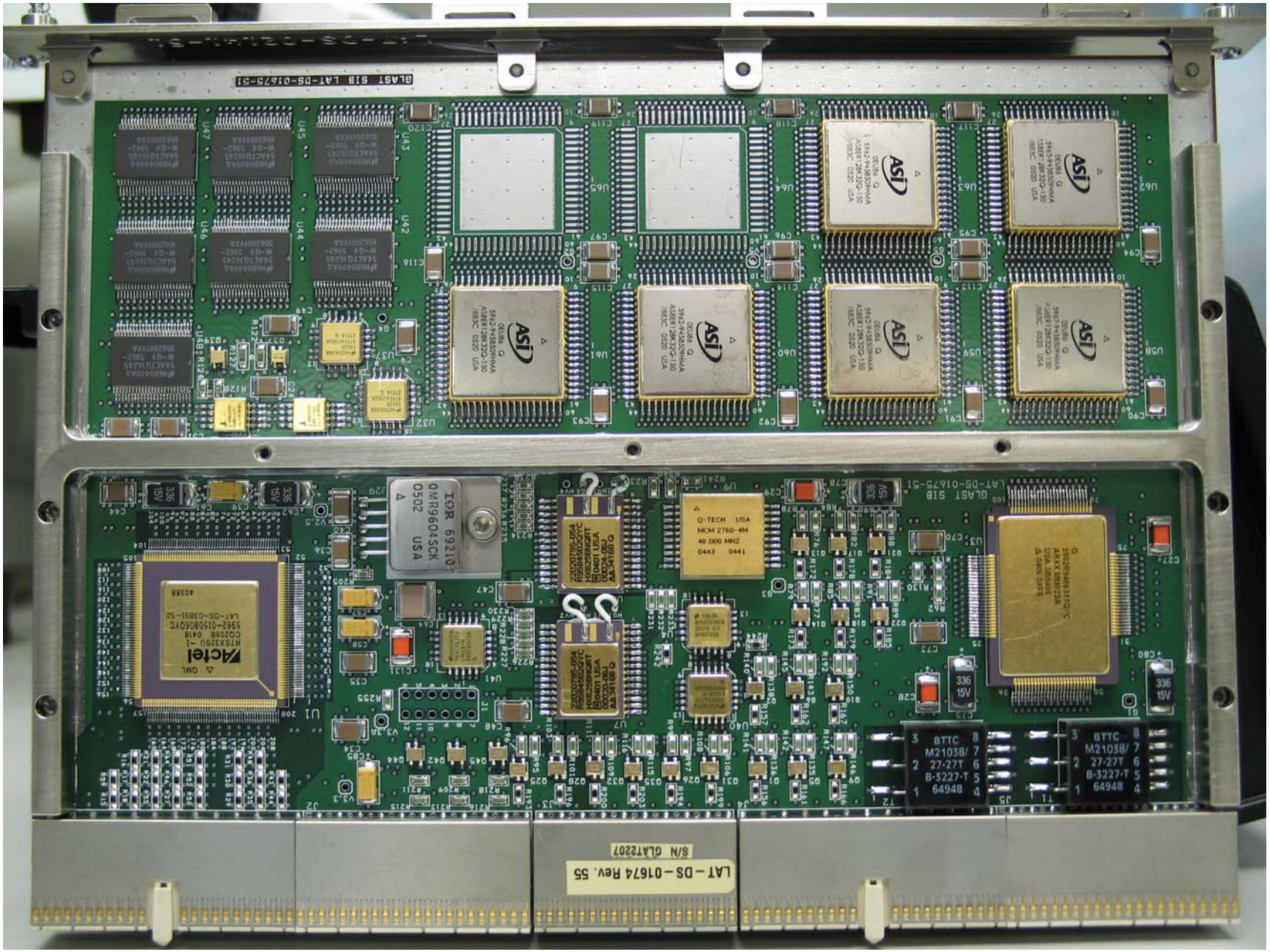

100G
teladrop
100G
50G
teladrop
50G
25G
teladrop
25G


CAUTION
ELECTROSTATIC SENSITIVE DEVICES
CAUTION
FLIGHT
HARDWARE
HANDLE WITH CARE
LAT-DS-01674
S/N GLAT2207
PROTAPAK


100G
teladrop
100G
50G
teladrop
50G
25G
teladrop
25G

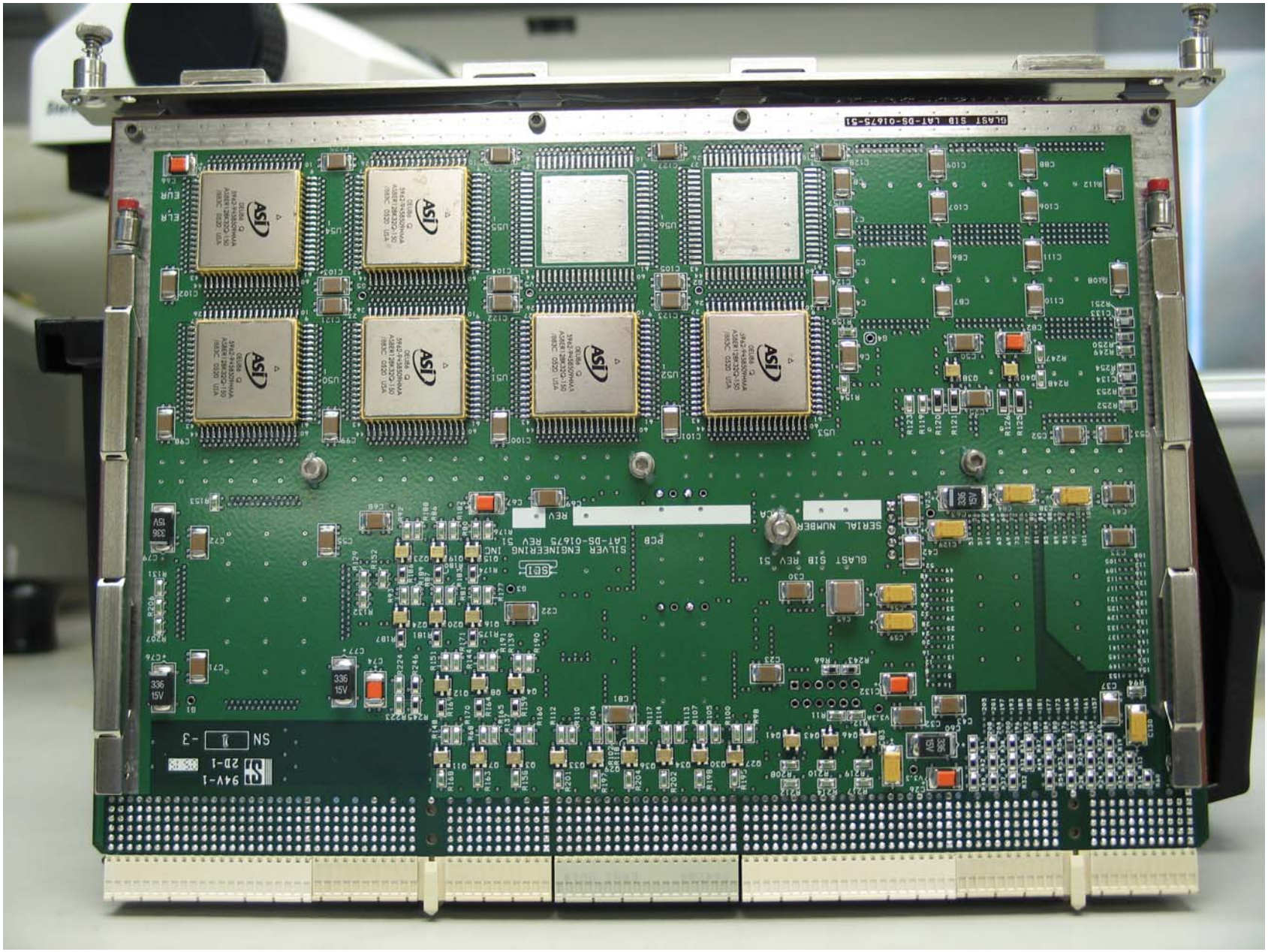
SN GLAT2207

PRE-TEST, IMG_1036.JPG



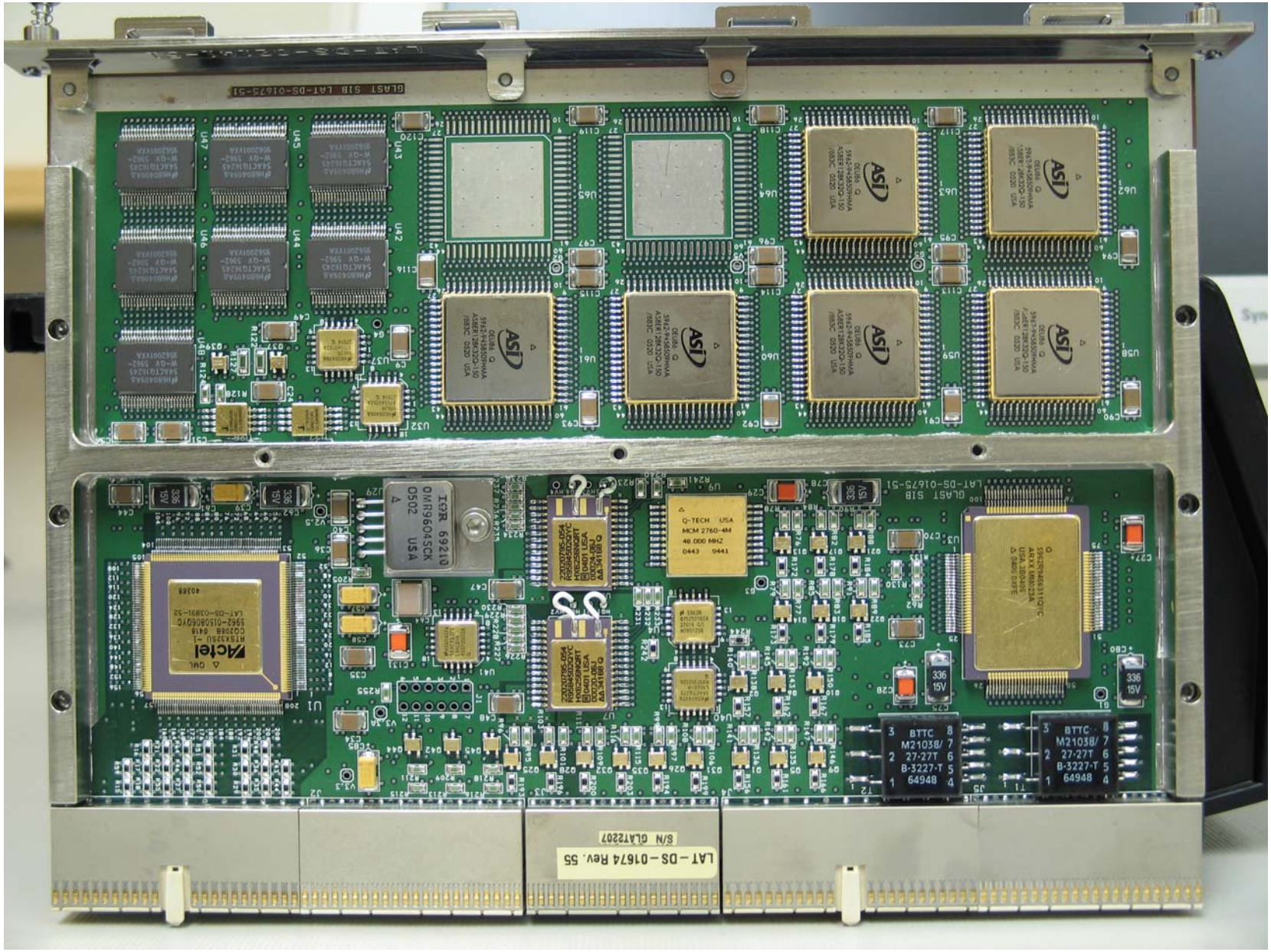
SN GLAT2207

PRE-TEST, IMG_1039.JPG



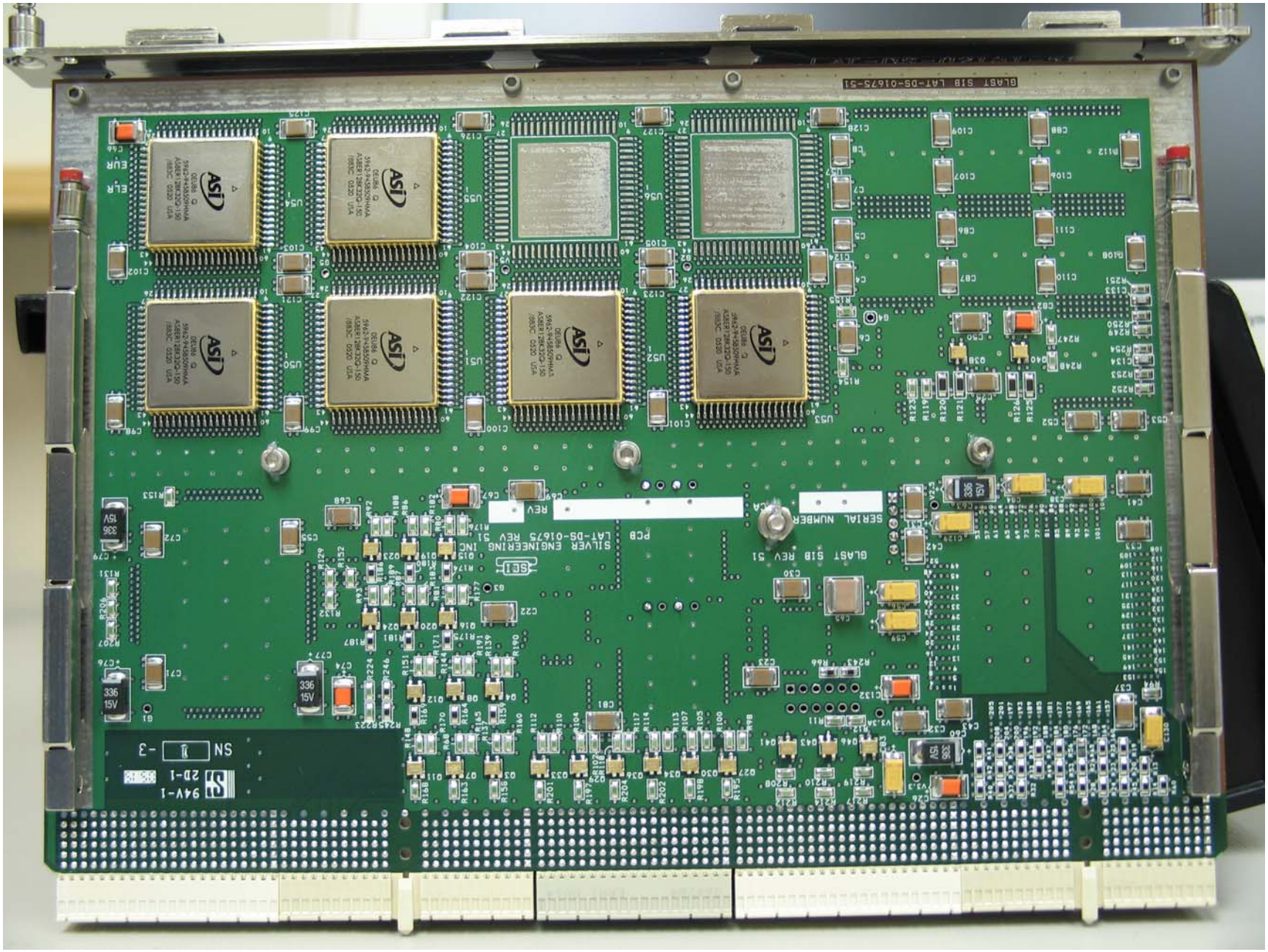
SN GLAT2207

POST-TEST, IMG_1067.JPG



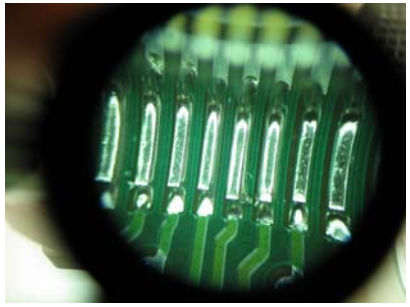
SN GLAT2207

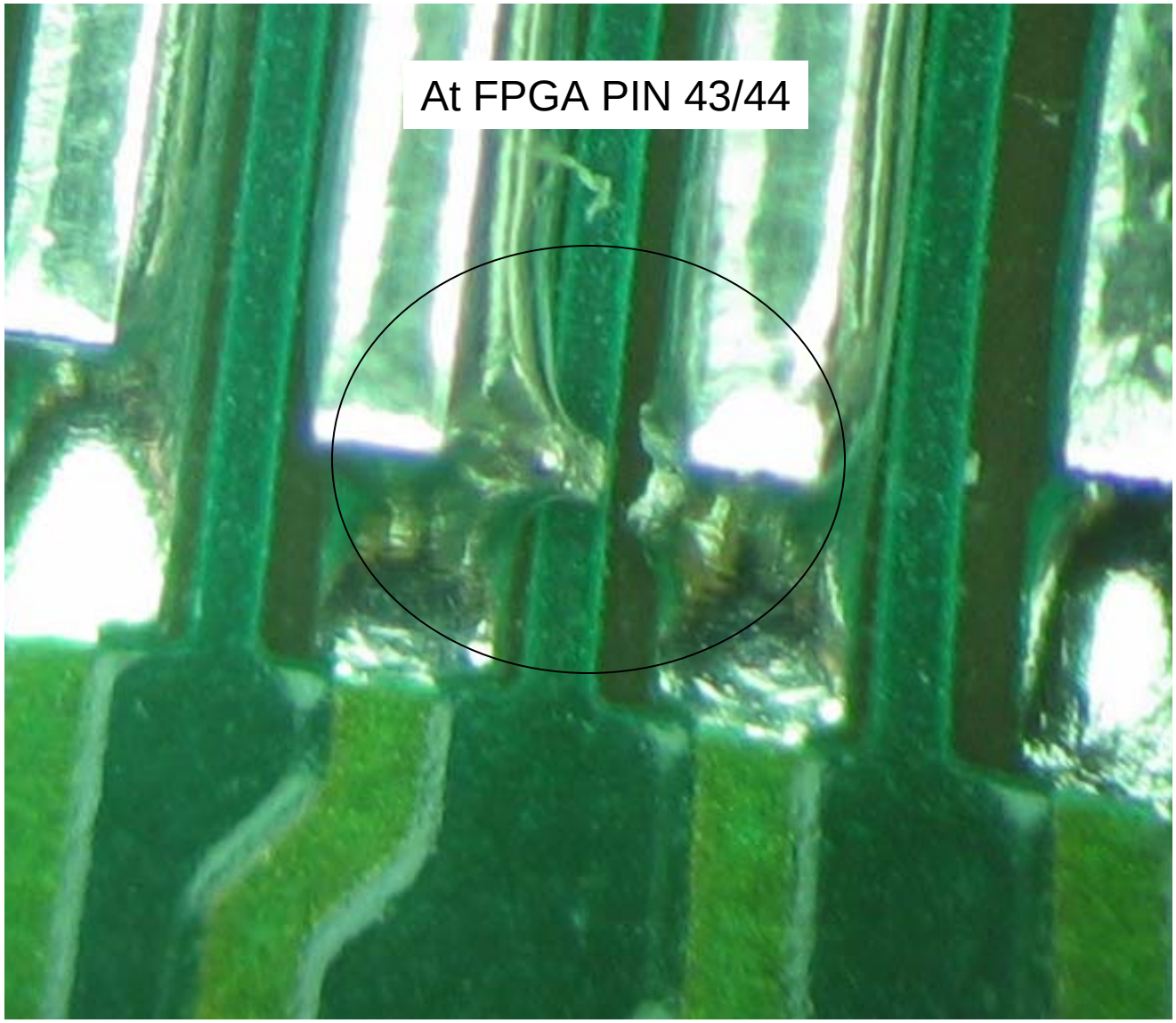
POST-TEST, IMG_1070.JPG



SN GLAT2207

WORKMANSHIP AREAS OF CONCERN





THE FOLLOWING IS FOR SIB SN GLAT2207, TEST PROCEDURE STEP 32

```
PCI:
PCI: dls
Script loaded!
PCI: run 1
PCI:  configuration setup for sib slot 6 card
PCI: w 8000000 c
08000000 :
08000004 : 2
08000008 :
0800000c :
08000010 : 22000000
08000014 : .
PCI:
PCI: w 8000048 c
08000048 : 200
0800004c : .
PCI:
PCI: m 8000000 c
08000000 : 084411aa
08000004 : 04000002
08000008 : ff000006
0800000c : 00000000
08000010 : 22000008
08000014 : 00000000
08000018 : 00000000
0800001c : 00000000
08000020 : 00000000
08000024 : 00000000
08000028 : 00000000
0800002c : 00000000
08000030 : 00000000
08000034 : 00000000
08000038 : 00000000
0800003c : 00000100
08000040 : 00000000
08000044 : 00000000
08000048 : 00000200  .
PCI:
PCI: m 22000000
22000000 : 00000004
22000004 : 00000080  .
PCI:
PCI: m 22000004
22000004 : 00000080  0
22000004 : 00000000  .
PCI:
PCI: m 22000000
22000000 : 00000006
22000004 : 00000000
22000008 : 00000000
2200000c : 00000000
```

```
22000010 : 00000006
22000014 : 00000000  .
PCI:
PCI:
PCI: EOS
Script stopped!
PCI: m 08000000 c
08000000 : 084411aa
08000004 : 04000002
08000008 : ff000006
0800000c : 00000000
08000010 : 22000008
08000014 : 00000000
08000018 : 00000000
0800001c : 00000000
08000020 : 00000000
08000024 : 00000000
08000028 : 00000000
0800002c : 00000000
08000030 : 00000000
08000034 : 00000000
08000038 : 00000000
0800003c : 00000100
08000040 : 00000000
08000044 : 00000000
08000048 : 00000200
PCI: dls
Script loaded!
PCI: run 1
PCI: -- SIB REGISTER TEST
PCI: -- TEST WRITTEN 11 JULY 2005
PCI: PAUSE
Press any key to continue...
PCI: -- WATCH DOG TIMMER TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
PCI: M 22000000
22000000 : 00000006
22000004 : 00000000
22000008 : 00000000
2200000c : 00000000
22000010 : 00000006  0
22000010 : 00000002  .
PCI:
PCI: M 22000000
22000000 : 00000002  .
PCI:
PCI: --WAIT 60SEC  ADDRESS 22000000 SHOULD BE = 00000002
PCI: wait 60000
PCI: M 22000000
22000000 : 00000002  .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 00000002
PCI: --WAIT 6SEC
```

```
PCI: wait 6000
PCI: M 22000000
22000000 : 00000006  .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 00000006
PCI: --END OF WDT TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
PCI:
PCI:
PCI: ---------------------------------------------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: -- SUMMIT RESET TEST
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000000  80
22000004 : 00000080  .
PCI:
PCI: M 22000000
22000000 : 00000004  .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 00000004
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000080  0
22000004 : 00000000  .
PCI:
PCI: M 22000000
22000000 : 00000006  .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 00000006
PCI: PAUSE
Press any key to continue...
PCI:
PCI: --END OF SUMMIT RESET TEST
PCI:
PCI:
PCI:
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
```

```
PCI:
PCI:
PCI: ----------------------------------------------------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: EEPROM WRITE ERROR TEST
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006  .
PCI:
PCI: --ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: M 22800000
22800000 : ffffffff  12345678
22800000 : ffffffff  .
PCI:
PCI: M 22000000
22000000 : 00000046  .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 46
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006  .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: M 22C00000
22c00000 : ffffffff  87654321
22c00000 : ffffffff  .
PCI:
PCI: M 22000000
22000000 : 00000086  .
PCI:
PCI: --  ADDRESS 22000000 SHOULD BE = 86
PCI: PAUSE
Press any key to continue...
PCI: M 22000000
22000000 : 00000006  .
PCI:
PCI: -- ADDRESS 22000000 SHOULD BE = 6
PCI: PAUSE
Press any key to continue...
PCI: END OF WRITE ERROR TEST
PCI: PAUSE
Press any key to continue...
PCI:
PCI:
PCI:
```

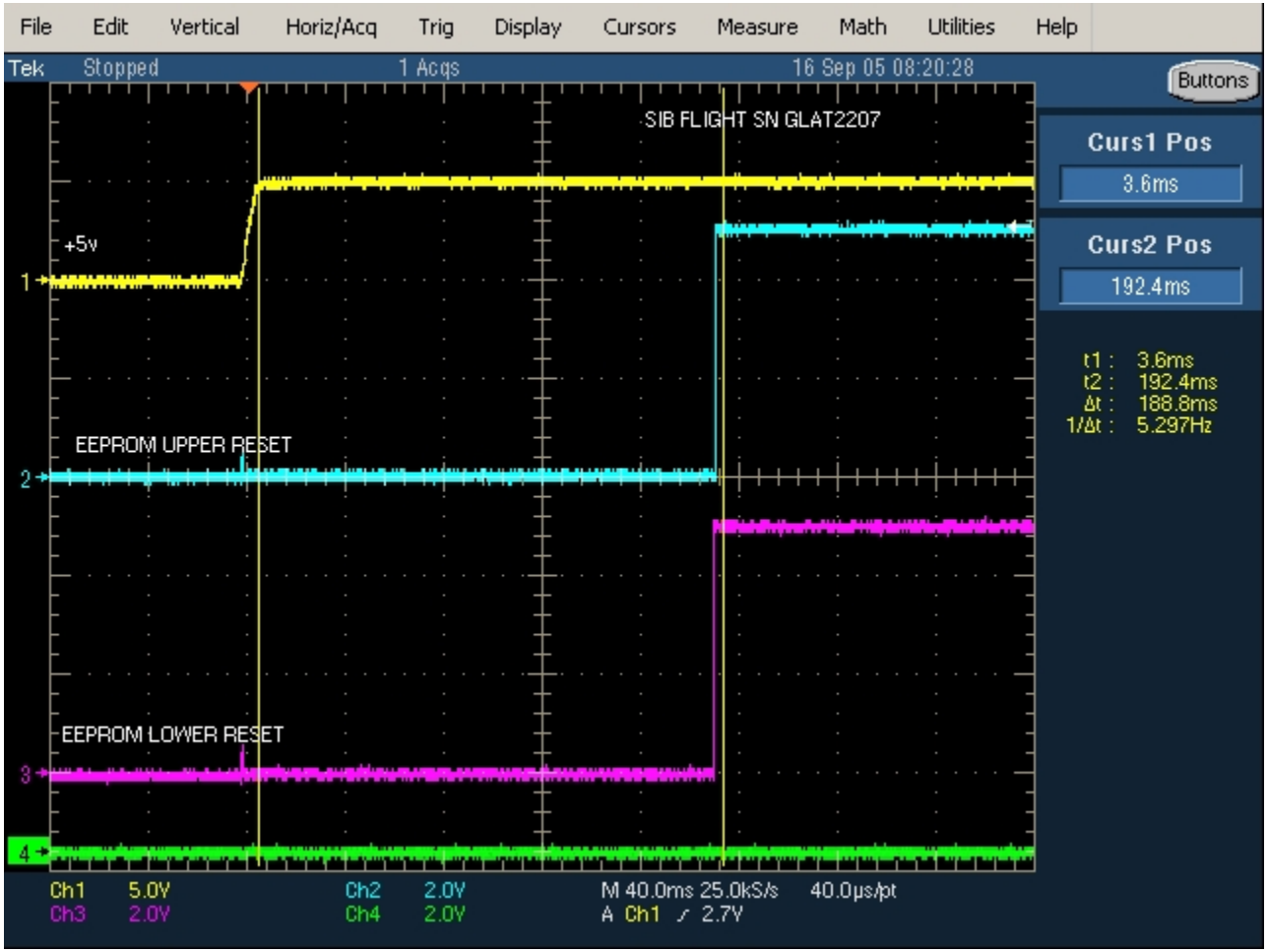
```
PCI:
PCI: ----------------------------------------------------
PCI:
PCI:
PCI:
PCI:
PCI:
PCI:
PCI: SOFTWARE INTERRUPT TEST
PCI: PAUSE
Press any key to continue...
PCI: M 08000048 C
08000048 : 00000200  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 200
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000000  40
22000004 : 00000040  .
PCI:
PCI: M 08000048 C
08000048 : 00000300  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 300
PCI: PAUSE
Press any key to continue...
PCI: M 08000048 C
08000048 : 00000300  300
08000048 : 00000200  .
PCI:
PCI: M 08000048 C
08000048 : 00000200  .
PCI:
PCI: -- CONFIGURATION ADDRESS 08000048 SHOULD BE = 200
PCI: PAUSE
Press any key to continue...
PCI: M 22000004
22000004 : 00000040  0
22000004 : 00000000  .
PCI:
PCI: -- END OF REGISTER TEST
PCI: EOS
Script stopped!
PCI:
```

END OF SCREEN CAPTURE FOR TEST PROCEDURE STEP 32

SN GLAT2207

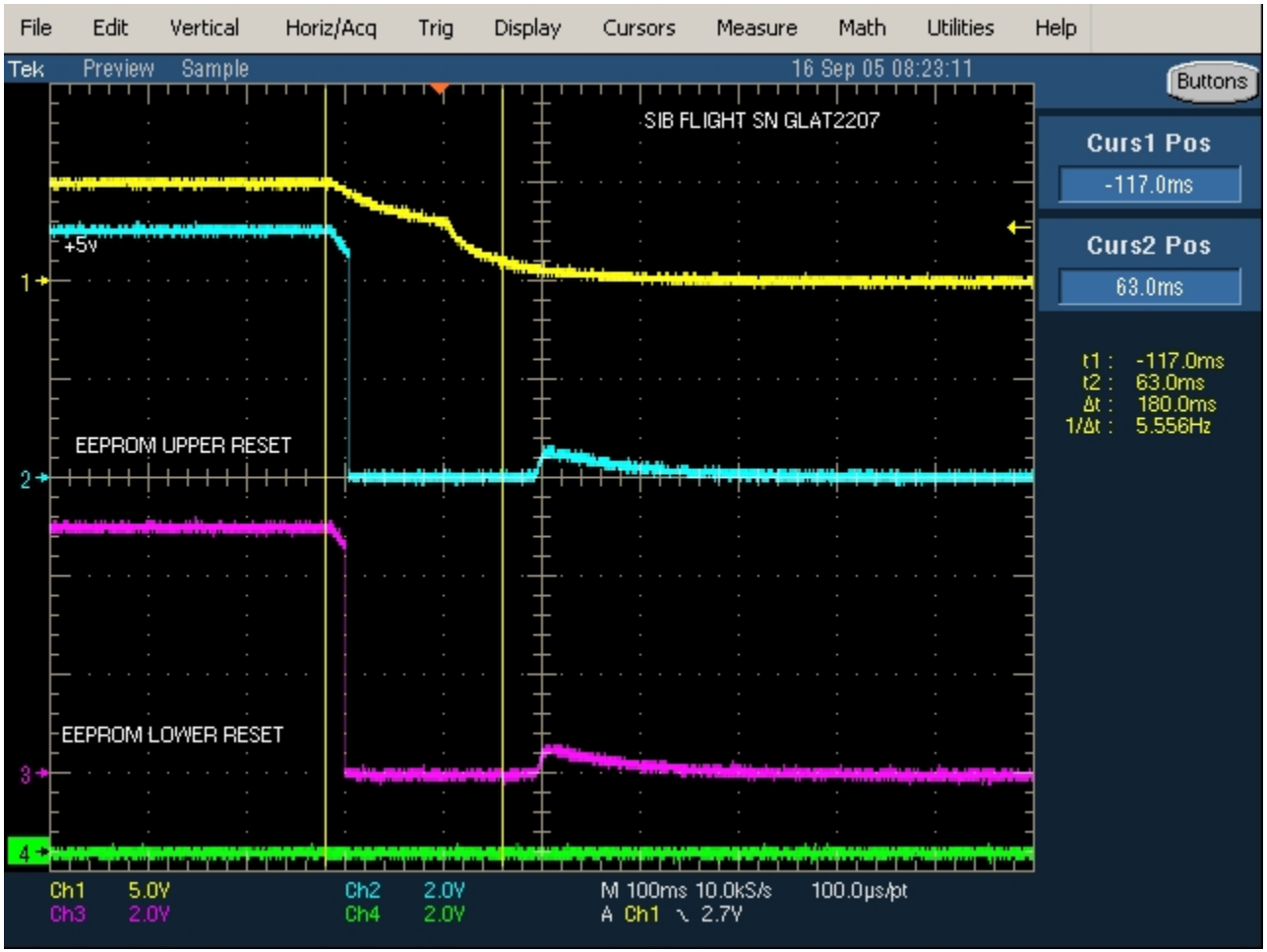
SN2207 STEP26D.jpg

SN GLAT2207

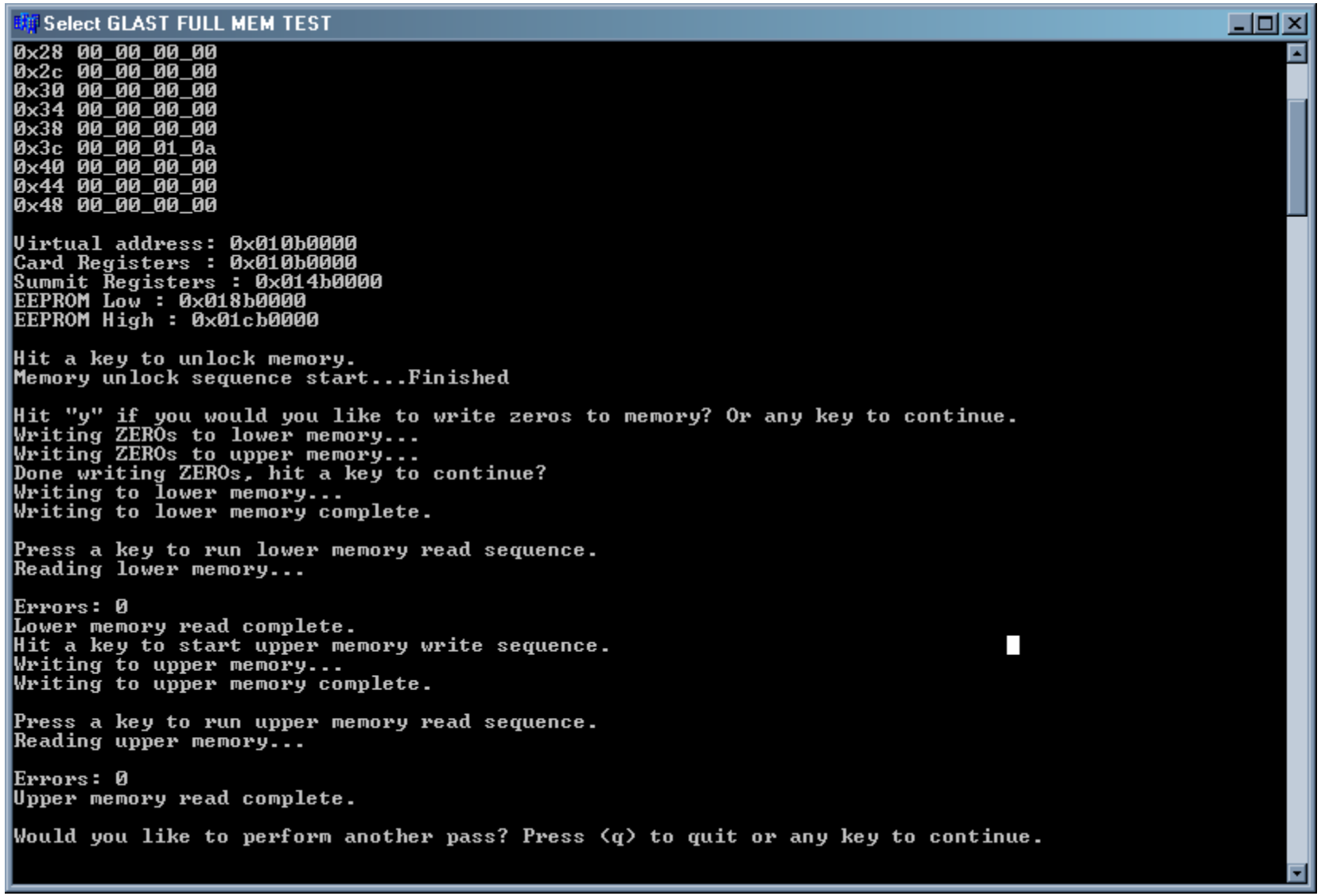


SN2207 STEP121C4.jpg

SN GLAT2207



SN2207 STEP121D4.jpg


Select GLAST FULL MEM TEST
0x28 00_00_00_00
0x2c 00_00_00_00
0x30 00_00_00_00
0x34 00_00_00_00
0x38 00_00_00_00
0x3c 00_00_01_0a
0x40 00_00_00_00
0x44 00_00_00_00
0x48 00_00_00_00
Virtual address: 0x010b0000
Card Registers : 0x010b0000
Summit Registers : 0x014b0000
EEPROM Low : 0x018b0000
EEPROM High : 0x01cb0000
Hit a key to unlock memory.
Memory unlock sequence start...Finished
Hit "y" if you would you like to write zeros to memory? Or any key to continue.
Writing ZEROs to lower memory...
Writing ZEROs to upper memory...
Done writing ZEROs, hit a key to continue?
Writing to lower memory...
Writing to lower memory complete.
Press a key to run lower memory read sequence.
Reading lower memory...
Errors: 0
Lower memory read complete.
Hit a key to start upper memory write sequence.
Writing to upper memory...
Writing to upper memory complete.
Press a key to run upper memory read sequence.
Reading upper memory...
Errors: 0
Upper memory read complete.
Would you like to perform another pass? Press (q) to quit or any key to continue.

Select GLAST READ MEM ONLY TEST

```
Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press <q> to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press <q> to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press <q> to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
Reading upper memory...

Errors: 0
Upper memory read complete.

Would you like to perform another pass? Press <q> to quit or any key to continue.

Press a key to run lower memory read sequence.
Reading lower memory...

Errors: 0
Lower memory read complete.

Press a key to run upper memory read sequence.
```

SIB MATE AND DE-MATE LOG SHEET

SIB SN2207

Note: The SIB card only has the CPCI bus connectors.

Mate or De-Mate	Where	Date	Comment
Mate	SIB Test fixture slot 5	15SEPT2005	Wrong slot
De-Mate		15SEPT2005	Verified ok
Mate	SIB Test fixture slot 6	15SEPT2005	
De-Mate		19SEPT2005	

SIB EEPROM WRITE CYCLE LOG SHEET

SIB SN2207

Number of writes	Address	Page or single	Who/when	Running Balance
1	22987000	Single	D. Silver 15sept05	1
1	22d87000	Single	D. Silver 15sept05	1
12	1 unique address/chip	Single	D. Silver 15sept05	1
1	All memory	Page	D. Silver 15sept05	2