LAT ASSEMBLY AND INSPECTION DATA Record #1124

LAT Assembly Information:
Equipment Title: PDU CCA pre-conformal coat rework.
Reference Designator: LAT-DS-01696

LAT-DS-01696 55 GLAT - P. YOUNG

Subsystem: Electronics and Data Acquisition
Equipment Class: Flight
Prepared by: P. YOUNG

Approvals:
Responsible Engineer: P. YOUNG
Date Signed: 5/10/05

 Manufacturing Engineer: R. PATTERSON
Date Signed: 5/10/05

Quality Engineer: J. CULLINAN
Date Signed: 5/11/05

Step Instructions:

10 This AIDS documents reworking the PDU CCA prior to conformal coating.

UNIT IS TO BE HANDLED USING FLIGHT HARDWARE.
OBSEVE PRECAUTIONS TO PREVENT ESD OR PHYSICAL DAMAGE. PER LAT-TD-0279-01, PERFORM ALL OPERATIONS IN B/35 CLEANROOM.

30 Issue qty = 2 capacitors CDR31B3X473AKUS, LOT # 5/10/05

40 Remove both PDU CCAs simultaneously from PDU housing. Retain fasteners.

50 Issue wire MS18226-6-A-30-9. Record lot date 5/10/05

9:31:13

5/10/05

Solder 0.7" long wire to each end of each capacitor using solder lot and date code number. 5/10/05

9:22:56

5/10/05

Applied Flux to tin wires. Record flux number. Clean with Isopropyl Alcohol.

Solder one pigtailed capacitor CDR33B473AKUS to pin 1 of L5 and pin 1 (+) of C53, located on bottom side of one PDU PWB. See LAT-DS-02191-59 sheet 3 for orientation.

Repeat capacitor installation on second PDU PWB.

Clean soldered joints as required with alcohol to remove flux residue. Visually inspect for cleanliness.

QC inspect all solder work with microscope 10x.

Bond capacitors to PDU boards using Hysol 0151. The auto-mixing dispenser with two-part dispenser. Include hardness cup sample of Hysol with part during cure.

Cure Hysol for 2 hrs at 66 deg C in air. Verify shore hardness of cured sample.

QC inspect bonded components.

Reinstall both PDU CCAs simultaneously into PDU housing. Reuse fasteners.

Close this AIDS.  

---

**LAT ASSEMBLY AND INSPECTION DATA Record #1155**

### LAT Assembly Information:
- **Equipment Title**: GLAST
- **PDU Board Re-work**: Space
- **Reference Designator**: Electronics and Data Acquisition

### Approvers:
- **Responsible Engineer**: Guenther Halter
- **Manufacturing Engineer**: R. Patterson
- **Quality Engineer**: Y. Li

### Step Instructions:

<table>
<thead>
<tr>
<th>Step #</th>
<th>Step Instruction</th>
<th>Operator ID</th>
<th>Operator Date</th>
<th>Operator Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>This work order is to investigate problem on PDU Boards ID Number: GLAT1894, GLAT1895</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Lift Pin number 133 on FPGA Actel Reference number U3 on board ID Number GLAT1895 Refer To NCR 475</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Remove solder from U2 pin-133 Record solder lot and date code ________________ flux lot and date code ________________</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>QC to Inspect Pin lead</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Engineer to measure pin resistance from pin to pad</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Resolder pin to Pad</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>QA inspect re-soldered pin</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Remove FET Reference number Q1822 on board ID number: GLAT1895, Refer to NCR 476</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>QC to Inspect solder pads</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LAT ASSEMBLY AND INSPECTION DATA Record #1155

LAT Assembly Information:
- **Equipment Title**: GLAST
- **PDU Board Re-work**: Yes
- **Reference Designator**: 133
- **Drawing No.**: 00000000
- **Rev.**: A
- **Serial No.**: 00000000
- **Equipment Class**: Flight
- **Prepared by**: Lupe Salgado

Approvers:
- **Responsible Engineer**: Gujer Haller
- **Manufacturing Engineer**: R. Patterson
- **Quality Engineer**: Ye Liew

Step Instructions:

<table>
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<tr>
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<tr>
<td>10</td>
<td>This work order is to investigate problem on PDU Boards ID Number: GLAT1894, GLAT1895</td>
</tr>
<tr>
<td>20</td>
<td>Lift Pin number: 133 on FPGA Actel Reference number U3 on board ID Number: GLAT1895</td>
</tr>
<tr>
<td>30</td>
<td>Remove FET Reference number Q1S22 on board ID number: GLAT1895</td>
</tr>
<tr>
<td>35</td>
<td>Issue from Flight stores 2ea. 3K resistors part number: 976.42N6.</td>
</tr>
<tr>
<td>37</td>
<td>Add temporary 3K resistor from Source to Drain on FET M559-42K061</td>
</tr>
<tr>
<td>40</td>
<td>Q1S23 on board Id Number: GLAT1895</td>
</tr>
<tr>
<td>50</td>
<td>OC to inspect soldering</td>
</tr>
</tbody>
</table>


5/16/2005
Assemble and Inspection Data Sheet

Issue from flight stores 2ea. 976 ohms resistors part number M55342K06B976DR. 976 ohms 1/4 record lot and date code.

35. Perform test to troubleshoot. Pan resistor, No. 476. TC to inspect soldering and photograph.

36. Add temporary 3k resistors from GR to DIN on flight, reference number 41522 on board ID. Number: GLAT1895.

37. Replace resistor 3k and do test.

41. Perform test to troubleshoot. Pan resistor, No. 476. TC to inspect soldering and photograph.

51. Solder the replacement resistor. It is to be into the GRAT 1895. Lot No. LIA 418.

52. DA inspect and photograph.

53. Touch up damaged traces of the 3k Ohm resistor. Lot No. 241C12544. Exp date 4/15/86.

55. Install FMA, C10, C11, C12 into PDW enclosure. Following enclosure modification:

56. Remove the 3k resistor. It is to be into the GRAT 1895. Lot No. LIA 418.

60. Replace with newly boxed resistors. Work to be performed in both COAX.

61. Replace with newly boxed resistors. Work to be performed in both COAX.


SFC: Plate kedge type

Factor: 5/5
60 - Issue from Flight Stores M5F342408927068287
   DATE code: 01345

61 - Issue from Flight Stores M5F342408927101487
   DATE code: 01515.
# LAT ASSEMBLY AND INSPECTION DATA Record #1230

## LAT Assembly Information:
- **Equipment Title:** GLAT1898
- **Subsystem:** Electronics and Data Acquisition
- **Rev:** Flight
- **Serial No.:**

## Approvers:
- **Responsible Engineer:**
  - **Name:** Gunther Muller
  - **Date Signed:**

- **Manufacturing Engineer:**
  - **Name:** R. Patterson
  - **Date Signed:**

- **Quality Engineer:**
  - **Name:** Y.C. Liew
  - **Date Signed:**

## Step Instructions:

<table>
<thead>
<tr>
<th>Step</th>
<th>Step Instruction</th>
<th>Operator ID</th>
<th>Operator Date</th>
<th>Operator Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>This work order is to continue Re-work on PDU-BOX Serial number: GLAT1898 per NCR# 4769</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Issue 50ca. from Flight Stores resistor 49.9k M55:42K06B-49E9R</td>
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</tr>
<tr>
<td>30</td>
<td>Issue 46ca. from Flight Stores resistor 100K M55:42K06B-100ER</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Issue 12ca. from Flight Stores resistor 301K M55:42K06B-301ER</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On PDU boards serial number GLAT1894 and GLAT1895
Remove the following resistors:

---

<table>
<thead>
<tr>
<th>Location 1</th>
<th>Location 2</th>
<th>Location 3</th>
<th>Location 4</th>
<th>Location 5</th>
<th>Location 6</th>
</tr>
</thead>
</table>

QC to inspect solder pads 6/31/05

Solder 49.9k M55342K06B49E9R in the following locations:
R501, R504, R507, R510, R512, R516, R519, R522, R525, R528, R531, R534, R537, R540, R543, R546, R549, R552, R555, R558, R561, R564, R567, R570, R573, R576, R577

Record solder lot 5/1/05

QC to inspect final soldering

6/1/05
GLAST
The Gamma Ray Large Area Space Telescope

LAT ASSEMBLY AND INSPECTION DATA Record #1127

LAT Assembly Information:
Equipment Title
PDU BOX, IN PROCESS THERMAL CYCLE AND ELECTRICAL PERFORMANCE TESTING AT SLAC

Reference Designator

Drawing No. LAT-DS-01696
Rec. 58
Serial No. GLAT-14777

Subsystem Electronics and Data Acquisition
Equipment Class Flight
Prepared by P. YOUNG

Approvers:
Responsible Engineer P. YOUNG
Date Signed: 5-11-05

Manufacturing Engineer R. PATTERSON
Date Signed: 5-11-05

Quality Engineer Y. C. LIEW
Date Signed: 5-11-05

S. Instructions:
Step# Step Instruction Operator ID Operator Date Operator Stamp

10 The purpose of this work order is to receive an in-process PDU Box for thermal cycling and pre and post thermal cycle electrical performance testing. Upon successful completion of this work order, unit will be shipped back to Aeroflex to complete installation of flight hardware into box and conformal coating.

UNIT IS TO BE HANDLED USING FLIGHT HARDWARE PRECAUTIONS TO PREVENT ESD OR PHYSICAL DAMAGE PER LAT-03797-01.

20 Perform incoming inspection of shipping container and shock monitors. QA verify and report.

30 QC visually inspect PDU housing and CCAs within.

Install connector savers on all connectors. Record on mate/demate log.


50 5/10/2005
Perform Electrical Interface Continuity and Isolation Test per LAT-TD-04332-04.

Perform CCA Test per LAT-TD-02544-02. Skip sections 5.2.5 and 5.2.6. Subsequent steps of this AIDS replaces the skipped section.

Perform Stray Voltage Test per LAT-TD-04351-01.

Perform Performance Test per LAT-TD-01744-02. Stop the test at 5.2.9.1 step 50. Turn all electronics off. Attach thermocouple to PDU case and route out of chamber to DVM.

Engineering and QA review and approve performance test data pre thermal cycling.

Perform thermal cycle, 3 cycles, between -40°C and +55C with a minimum 15 minute soak at each temperature. The rate of change in temperature shall not exceed 5°C per minute. The thermal chamber shall be continuously purged with clean dry air or gaseous N2 to prevent water condensing in the chamber and on the PDU unit. Cycling shall start at ambient then increase to the high temperature for the first soak, then continue for 3 cycles. Proceed to next AIDS step.

Commence a 4th temperature cycle. Stop at +55°C and soak for 15 minutes. Execute LAT-TD-01744-02 section 5.2.9.1 step 53-54. When done with the test turn all electronics off. Proceed to next AIDS step.

Continue the temperature cycle upwards -40°C. Stop at +40°C and soak for 15 minutes. Execute LAT-TD-01744-02 section 5.2.9.1 step 53-54. When done with the test turn all electronics off. Finish the temperature cycle with a 30 minute cool down period at 25°C. Proceed to next AIDS step.

Open the temperature chamber and perform LAT-TD-01744-02 section 5.2.9.2 steps 1-10.

Close the temperature chamber.

Commence a 5th temperature cycle. Stop at +55°C and soak for 15 minutes. Execute LAT-TD-01744-02 section 5.2.9.2 step 2-10. When done with the test turn all electronics off. Proceed to next AIDS step.

Continue the temperature cycle towards -40°C. Stop at -40°C and soak for 15 minutes. Execute LAT-TD-01744-02 section 5.2.9.2 step 2-10. When done with the test turn all electronics off. Finish the temperature cycle with a 30 minute cool down period at 25°C. Proceed to next AIDS step.

Technicians to record temperature chamber name, model #, and calibration dates. QA verify.

COPY OF THERMAL CYCLE PROFILE TO WORK ORDER.

Engineering and QA review and approve performance test data obtained during thermal cycles.

Perform Performance Test per LAT-TD-01744-02. Stop the test at 5.2.9.1 step 4-8. Turn all electronics off.

Engineering and QA review and approve performance test data post thermal cycling.

Remove connector savers. Responsible engineer to bag and identify for later use with remaining production PDU units. Update the MATE/DEMATE LOG.

Responsible engineer to retain work order binder with data.

QC inspect PDU unit.

Package unit in ESD resistant bag and packaging. Pack for shipment per LAT-MD-00473.

QC to ensure that shock monitors have been reset.

http://www.bluekiss.stanford.edu/documents/Assembly/assembly_test_plan/assembly_id41722 5/10/2005
LAT ASSEMBLY AND INSPECTION DATA Record #1127

LAT Assembly Information:
Device Title: LAT-DS-01696

Ref No.:

Serial No.:

Draw:

례:

그리

Reference Designator:

Subsystem:

Electronics and Data Acquisition

Equipment Class:

Flight

Prepared by:

P. YOUNG

Approvers:

Responsible Engineer:

Manufacturing Engineer:

R. PATTERSON

Quality Engineer:

Y. C. LIEW

Date Signed:

Date Signed:

-----

Step# Step Instruction

10 The purpose of this work order is to receive an in process PDU Box for thermal cycling and pre and post thermal cycle electrical performance testing. Upon successful completion of this work order, unit will be shipped back to Aeroflex to complete installation of flight hardware into box and conformal coating.

15 Issue from Flight Stores 16ea. Screws#6 part number NAS1352N06-6 Label bag and deliver to clean room.

20 UNIT IS TO BE HANDLED USING FLIGHT HARDWARE PRECAUTIONS TO PREVENT ESD OR PHYSICAL DAMAGE PER LAT-TD-02797-01.

30 Perform incoming inspection of shipping container and shock monitors. QA verify and report.

40 QC visually inspect PDU housing and CCAs within.


6/1/2005
Install connector savers on all connectors. Record on mating/break log.

Perform Electrical Interface Continuity and Isolation Test per LAT-TD-04332-04.

Perform CCA Test per LAT-TD-02544-02. Skip sections 5.2.5 and 5.2.6. Subsequent steps of this AIDS replace the skipped section.

Perform Stray Voltage Test per LAT-TD-04840-03.

Repair/rework per AIDS 155.125.1 (GLAT1895-01 pin 133, replace Q15222) (GLAT1894 and GLAT1895: R13-14, R604-605) (box machining, kapton tape) (turn off swap JS 16).

Retest the following for STM following repairs: LAT-TD-04332-04 5.2.3.1.2, 5.2.2.1.2, 5.2.4.1.2, 5.2.4.1.2.1, 5.2.4.2.2, 5.2.5.2.1, 5.2.6.4.2, 5.3.4.1.2, 5.3.4.1.2.1, 5.3.4.1.2.2, 5.2.3.3 STEP 6, 5.2.4 STEP 1-10, STEP 19-26 LAT-TD-04340-03 5.3.6, 5.3.8, 5.3.8, 5.3.8 (JS10 ONLY), 5.3.8.2 (JS16 ONLY).

Perform Performance Test per LAT-TD-01744-02. Stop the test at 5.2.9.1 step 48. Turn all electronics off. Attach thermocouple to PDU case, PDU FPGA, PDU board and route out of chamber to 3 DVMs.

Perform thermal cycle, between -40℃ and +55℃ with a minimum 15 minute soak at each temperature. The rate of change in temperature shall not exceed 5℃ per minute. The thermal chamber shall be continuously purged with clean dry air or gaseous N2 to prevent water from condensing in the chamber and on the PDU unit. Cycling shall be maintained in high temperature for the first soak following profile of next AIDS STEPS. Proceed to next AIDS STEPS.

Bring oven to +55℃ and soak for 30 minutes. Execute LAT-TD-01744-02 section 5.2.9.1 step 14 at (28V, 3.6V, 40MHz), (28V, 3.6V, 40MHz), (28V, 3.6V, 25MHz), (28V, 3.6V, 20MHz), (28V, 3.6V, 10MHz). Record FPGA temperature from DVM.

Note: Q15222 is disconnected from 06720 during register tests since Q15222 is connected to 06720 only when doing 6.2.9.2, step 21-21 and 5.2.9.1 step 21-21 only turn on the load at 21-21.

http://www-glass.instac.stanford.edu/documents/Assembly/assembly_record.asp?id=14472
Perform LAT-TD-017444-02 section 5.2.9.1 step 54. Perform LAT-TD-01744-02 section 5.2.8.2 steps 3-21, only TEMS-11 will pass because only those loads are connected in the test setup. Do these tests at (25V, 3.0V, 40MHz) and (28V, 3.0V, 40MHz).

Execute LAT-TD-017444-02 section 5.2.8.1, one set of "Point Extraction" and "Verify Linearity" test. Nominal v and eik. Proceed to next AIDS step.

Continue the temperature cycle towards -40C. Stop at -40C and soak for 30 minutes minimum. Execute the tests of step 115 of this AIDS.

Execute the tests of step 120 of this AIDS.

Execute the tests of step 125 of this AIDS.

When done with the test turn all electronics off. Finish the temperature cycle with a 20 minute cool down period at 25C. Proceed to next AIDS step.

Perform Tests of step 115 of this AIDS. Turn all electronics off.

Record FPAA temperature.

Technician to record temperature chamber name, model #, and calibration dates. QA verify.

COPY OF THERMAL CYCLE PROFILE TO WORK ORDER.

Repair/rework per AIDS 1-2-5-6-7 (GLAT1894 and GLAT1895: overload resistor changes)

React the following for STM following repair: LAT-TD-04332-04 5.2.2.1, 2.5.2.2, 2.2.1-2.1-3, 5.2.1, 2.5.2.2, 2.5.3.6, 2.5.4-115.2 LAT-TD-04334-04 5.2.3.1, 5.3.7, 5.3.3.1, 5.2.6-115.5 LAT-TD-04335-05 5.2.6, 5.3.7, 5.3.3.1 (ULD ONLY), 5.3.9, 5.1 (UL13 ONLY)


6/1/2003 10:27:35
6/1/2003 10:26:00
6/1/2003 10:30:44
6/1/2003 10:31:11
6/1/2003 10:33:2
6/1/2003 10:32:00
205  Repeat LAT-TD-01744-02 5.2.1, 5.2.4, 5.2.6 6-2-05

210  Engineering and QA review and approve performance test data. 6/1/00

220  Remove connector savers. Responsible engineer to bag and identify for later use with remaining production PDU units. Update the MATE/DE-MATE LOG. N/A

230  Responsible engineer to retain work order binder with data.

240  QC inspect PDU unit. 6/1/05

250  Package unit in ESD sensitive bag and packaging. Pack for shipment per LAT-MD-00473. 6-2-05

260  QC to ensure that shock monitors have been reset. 6/2/05

270  Ship to: Aeroflex, Colorado Springs 4350 Centennial Blvd Colorado Springs, CO 80907 Attn: John Norris 6/2/05

280  Close this AIDS.

1. 0:25:47 - 02
   5 - 12 - 05
   p 47
   step 5 77V NO resistance factor change to 80V

2. 0:25:40 - 02
   0 - 30
   0 - 34
   0 - 32
   0 - 40
   0 - 40
   0 - 32
   0 - 34
   0 - 30
   0 - 34
   0 - 32
   0 - 40
   0 - 40

3. 0:25:44 - 02
   p 30 step 26 0.0V -> 0.4V (3.043) 25%
   step 32 0.0V -> 0.4V (3.063)
   0:25:44 - 02

4. make sure flight harness does not obstruct screw access tube at JL 4 to MBX terminals. (ront board)

5. 0:02:127 - redline to remove C38
   0:02:304
   also see as NCR and additional step in work order

6. TP - 04384-03 redline p14, 116, 117, 119
data sheet
   limits for measure.... lines change to account for presence of 0.4 - 0.7 V on 28V bus after main feed switch.
   This is due to added overcurrent circuit in BLT box which is not present in 66E box.

   Data 1) M55G prior to GND ~ 7.7k 0.05V 0.43V
     M55G after to GND ~ 6.1k 0.63V 0.40V
     7.7k in to GND ~ 9.0k
     7.75 ohm in to GND ~ 9.0k
   Also new in circuit which affects V:
   out driven.
   28V -> 28V
Possible Redline

Possible Redline

Possible Redline

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P
12 need to open up range on spread
expected values - Brian says he did
the counts and he will
fix to use the existing
13
14 Temp cal script now accounts for
15 account for EICU and EICU
16 see CRT data sheet p. 146.
LAT ASSEMBLY AND INSPECTION DATA Record #1427

LAT Assembly Information:

Equipment Title: PDU BOX, PROTO-FLIGHT TESTING AT SLAC
Reference Designator: Electronics and Data Acquisition

Drawing No: LAT-DS-01696
Serial No: GLAT1898

Approvals:

Responsible Engineer: P. YOUNG
Date Signed: 7/20/20

Step Instructions:

The purpose of this work order is to perform Proto-Flight Testing on the first PDU Box that is a candidate for FLIGHT. This testing will include Safe-To-Mate testing, Performance testing, Vibration testing, Thermal Cycling, Mass/CG measurements, Thermal-Vacuum testing, and EMI testing.

10. Unit to be handled using Flight hardware precautions to prevent ESD or physical damage per LAT-1D-02797.

20. Issue from Flight Stores connector savers: (i) 940-004M1S-355, (ii) MWDML-51US P1, (iii) MWDML-100US P1, (iv) DGB186MF, (v) DGBH78MF, (vi) DGBH266MF.

10. Issue Adhesive, RTV, DC6-1104 from Flight stores.

10. Issue Hysol 0151 from Flight stores.

Perform incoming inspection of shipping container, stock.

monitors, and PDU Box exterior. QA verify and report.

Remove lid and inspect interior of PDU Box for IDD and physical damage. This is a visual inspection for obvious damage. QA verify and report.

Issue from Flight stores lid LAT-DS-01847 (GLAT1898).

Install lid (GLAT1898) per note 9 of LAT-DS-01696-59. Torque wrench ID#92406, cal due 12-15-05, set to 8-16 lbs.

Stake screws into lid using HySol 0151.

QA verify and report lid and screw installation. Deliver PDU to engineering for test.

Remove dust covers from PDU. Bag and save dust covers. Install connector savers on all PDU Box connectors. See step 30 for part #s. Record mates in the Mate/Demate Log.

Perform Electrical Interface Continuity and Isolation Test per LAT-TD-04332-05.

Perform Stray Voltage Test per LAT-TD-04384-04.

Perform Performance Test per LAT-TD-01744-03. In section 5.2.9.1 only setup equipment to do clock margining. Skip the setup for voltage margining and skip the setup of the Mux Brd. The equipment is setup on the testbench since the oven will not be used. Skip 5.2.9.1 steps 21-42. Skip 5.2.9.2. Record PDU "ON" time.

In LAT-TD-01744-03 section 5.2.4 repeat the Loads and Temp Sensor Mapping Test on the Prim GASU at clock frequencies [14MHz-21MHz, in 0.5MHz steps]. Refer to section 5.2.9 for setup of an external clock to the GASU. Attach data to data package of step 140 of this work order.

Measure voltage and current at power supply under no load.

conditions as follows: [only PDU0 on, only PDU1 on, only PDU0-GASU0 on, only PDU1-GASU1 on]. Use the Prim feed (JL3). Attach data and test setup information to data package of step 140 of this work order.

145
Engineering and QA review and approve Test Data thus far.

150
Remove connector savers from all PDU Box connectors. Record datum in the MateDemate Log. Bag and retain connector savers. Install dust covers on PDU Box connectors.

155
Perform Vibration Test per LAT-TD-06101.

160
Remove dust covers from PDU Box. Bag and save dust covers. Install connector savers on all PDU Box connectors. Record datum in the MateDemate Log.

165
Perform Performance Test per LAT-TD-01744-03. Skip sections 5.2.1, 5.2.6, and 5.2.7. In section 5.2.9.1 only setup equipment to do clock marging. Skip the setup for voltage marging and skip the setup of the mux board. The equipment is setup on the test bench since the oven will not be used. Skip 5.2.9.1 steps 21-42. Skip 5.2.9.2. Record PDU ON time.

170
Install PDU in oven and attach thermocouple to flange of PDU box. Route thermocouple wire out of oven to DVM.

175
Perform unpowered thermal cycling of PDU, 5 cycles, between -40C and +55C, 15 minute soak at each extreme, rate of temperature change < 5C per minute. Oven shall be continuously purged with clean dry air or pressurized N2 to prevent water condensation. Attach leg 3 of the thermocouple, complete graph attached. (Purpose is to verify conformance to performance over bench.)

180
Remove PDU from oven and remove thermocouple.

185
Perform Performance Test per LAT-TD-01744-02. Skip sections 5.2.5, 5.2.6, and 5.2.7. In section 5.2.9.1 only setup equipment to do clock marging. Skip the setup for voltage marging and skip the setup of the mux board. The equipment is setup on the test bench since the oven will not be used. Skip

Perform Performance Test per LAT-TD-01744-03. Skip sections 5.2.5, 5.2.6, and 5.2.7. In section 5.2.9.1 only setup equipment to do clock marging and skip the setup of the Max Box. The equipment is setup on the test bench since the oven will not be used. Skip 5.2.9.1 steps 21-42. Skip 5.2.9.2. Record PDU 'ON' time.

Record cumulative current draw as each load is turned on. Prim Feed with PDU 0 then 1. Rms Feed with PDU 0 then 1. Attach to data package of step 230.

Remove connector savers from PDU connectors except for IL3, JL5, JL7. Record diameters in the Mate/Demate Log. Bag and retain connector savers. Install dust covers on IL3, JL5, JL7 connector savers. Install EMI connector covers on all other PDU connectors. See LAT-TD-03639 for EMI connector cover part numbers.


Perform EMI Test per LAT-TD-03639. 9/23/05

Remove EMI connector covers. Bag and retain all covers. Remove connector savers on all PDU connectors. Record diameters in Mate/Demate Log. Install dust covers on all connectors.

Remove dust covers. Bag and retain all covers. Install connector savers on all PDU connectors. Record mates in Mate/Demate Log.

Perform Thermal Vacuum Test per LAT-TD-03639. Record PDU 'ON' time.

Perform Performance Test per LAT-TD-01744-03. Skip 5.2.9.1 only setup equip. to do clock marging. Skip voltage marging. Skip max. Read setup: No errors. Skip 5.2.9.1 steps 21-42. Skip 5.2.9.2. Record PDU 'ON' time. Attach final 'ON' time log to this work order.


8/15/2005
100 Engineering and QA review and approve Test Data.

310 Remove connector savers from all PDU Box connectors. Record demates in the Mate/Demate Log. Bag and retain connector savers for use on future Flight PDUs. Install dust covers on PDU box.

320 Remove PDU mounting flange screws and assemble flight versions. Do not install screws in places that interface with connector plate screws (4 places).

330 Per NCR #00389, complete staking of connector plate screws using Hysol 0151. QA inspect.

340 Determine mass/CG properties using LAT

350 Deliver PDU to I&T.
### LAT Assembly and Inspection Data

**Record #1583**

<table>
<thead>
<tr>
<th>Step #</th>
<th>Step Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td><strong>Issue Qty 16 P/N 9723-SS-0440 Jackposts from Flight Stores. Count and recount to insure only 46 have been issued. Record Qty Issued = 46.</strong></td>
</tr>
<tr>
<td>20</td>
<td><strong>Issue Qty 3 P/N 500-052-44-4 Jackposts from Flight Stores.</strong></td>
</tr>
<tr>
<td>30</td>
<td><strong>Issue Qty 49 P/N MS21643-04 from Flight Stores. Count and recount to insure only 49 have been issued. Record Qty Issued = 49.</strong></td>
</tr>
<tr>
<td>40</td>
<td><strong>Issue Qty 49 P/N NAS620C1 from Flight Stores. Count and recount to insure only 49 have been issued. Record Qty Issued = 49.</strong></td>
</tr>
<tr>
<td>50</td>
<td><strong>Remove Lid Screws and Lid from PDU (GLAT1898). Count all Lid Screws and bag/label them.</strong></td>
</tr>
</tbody>
</table>

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**Notes:**

INDIVIDUALLY REMOVE INCORRECT JACKPOST FROM PDU AND REPLACE WITH CORRECT PIN FOR EACH 49 PIN. REMOVE AND REPLACE ONE JACKPOST, WASHER AND NUT ASSEMBLY ONE AT A TIME. EXISTING WASHERS TO BE REUSED WITH NEW JACKPOSTS AND NUTS. TORQUE EACH POST TO 60 IN-OZ PER DRAWING 01696-61.

COUNT AND RECOUNT ALL REPLACED JACKPOSTS; NUT AND WASHERS. COUNTER MUST BE 49 EACH.

STAKE ALL NUTS USING HYSOL 0151.

QC INSPECT STAKING AND INSIDE OF PDU FOR LOOSE DEBRIS AND CONTAMINATION. CLEAN AS REQUIRED. 9-12-05

REINSTALL LID USING SCREWS. TORQUE TO 125 IN-0Z.

PERFORM ANY ADDITIONAL ELECTRICAL TESTING AS DIRECTED BY DAQ ENGINEERING. SIGN OFF SEQUENCE WITH N/A IF NO ADDITIONAL TESTS ARE REQUIRED. IF TESTING IS REQUIRED, UPDATE THIS AIDS SEQUENCE WITH DETAILS.

QC INSPECT 3-14-05

UPDATE NCR #634

CLOSE OUT WORK ORDER
LAT ASSEMBLY AND INSPECTION DATA Sheet for GLAST

LAT Assembly Information:  
Equipment Title: LAT ASSEMBLY AND INSPECTION DATA  
POU: LAT1898 REWORK PER NCR LAT-DS-01696-61  
Drawing No:  
Rec: 61  
Serial No: GLAT1898  
Prepared by: D. TARKINGTON

Reference Designator:  
Subsystem: Electronics and Data Acquisition  
Equipment Class: Flight  
Prepared by: D. TARKINGTON

Step Instructions:  

<table>
<thead>
<tr>
<th>Step</th>
<th>Instruction</th>
<th>Operator ID</th>
<th>Date</th>
<th>Stamp Update</th>
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</thead>
<tbody>
<tr>
<td>10</td>
<td>ISSUE QTY 46 P/N 9773-3S-0440 JACKPOSTS FROM FLIGHT STORES, COUNT AND RECOUNT TO INSURE ONLY 46 HAVE BEEN ISSUED, RECORD QTY ISSUED =</td>
<td></td>
<td>9/8/2000 AM</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>ISSUE QTY 3 P/N 500 052 4-4 JACKPOSTS FROM FLIGHT STORES</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>30</td>
<td>ISSUE QTY 49 P/N MS26043-04 FROM FLIGHT STORES, COUNT AND RECOUNT TO INSURE ONLY 49 HAVE BEEN ISSUED, RECORD QTY ISSUED =</td>
<td></td>
<td>9/8/2000 AM</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>ISSUE QTY 49 P/N NAS260C4 FROM FLIGHT STORES, COUNT AND RECOUNT TO INSURE ONLY 49 HAVE BEEN ISSUED, RECORD QTY ISSUED =</td>
<td></td>
<td>9/8/2000 AM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>REMOVE LID SCREWS AND LID FROM POU (GLAT1898), COUNT ALL LID SCREWS AND BAG/LABEL THEM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

9/28/2005
INDIVIDUALLY REMOVE INCORRECT JACKPOST FROM PDU AND REPLACE WITH CORRECT PIN FOR EACH 49 PC. REMOVE AND REPLACE ONE JACKPOST, WASHER AND NUT ASSEMBLY ONE AT A TIME. EXISTING WASHERS TO BE REUSED WITH NEW JACKPOSTS AND NUTS. TORQUE EACH POST TO 60 IN. OZ PER DRAWING 01096-61.

COUNT AND RECOUNT ALL REPLACED JACKPOSTS, NUT AND WASHERS. COUNT MUST BE 49 EACH.

STAKE ALL NUTS USING HY-SOL 0151.

QC INSPECT STAKING AND INSIDE OF PDU FOR LOOSE DEBRIS AND CONTAMINATION. CLEAN AS REQUIRED.

REINSTALL LID USING SCREWS. TORQUE TO 125 IN. OZ.

PERFORM ANY ADDITIONAL ELECTRICAL TESTING AS DIRECTED BY DAQ ENGINEERING. SIGN OFF SEQUENCE WITH N/A IF NO ADDITIONAL TESTS ARE REQUIRED. IF TESTING IS REQUIRED, UPDATE THIS AIDS SEQUENCE WITH DETAILS.

Remove dust covers from connectors. Install connector savers on all connectors and record in mate/demate log associated w/ WO1437.

Perform EICT per LAT-TD-04332-06.

Perform SVT per LAT-TD-04384-05.

Perform Load Board Mapping Test per LAT-TD-01744-04 section 5.2.4 but stop at step 20.

Use the GUI to turn on all TEM and EPU loads and record the current on the Xantrex PS.


9/30/2003
ASSEMBLY AND INSPECTION DATA SHEET

108 Repeat steps 105-106 of this WO and record if the test passed and the full load current on the Xantrex is the same as before.

109 Remove connector savers from all connectors and record in mate/demate log associated w/ WO1427. Install dust covers on connectors.

110 Stake lid screws with HYSOL 0151

120 QC Inspect

125 Update NCR #634

Mute flight cable to TDU JL31 for fit check. Remove flight cables. Record in mate/demate log of WO#1427. Update NCR 675.

Verify labeling on LAT-DS-01606 is at correct rev. Update drawings with labeling step if required. QA inspect.

130 Close out work order.


9/28/2005