**DOCUMENT CHANGE NOTICE (DCN)**

**ORIGINATOR:** Robert Johnson  
**PHONE:** 831-459-2125  
**DATE:** 1/10/03

**CHANGE TITLE:** DCN for LAT Tracker Subsystem Specification- Level IV Readout Electronics Requirements

**ORG.:**

<table>
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<th>TITLE</th>
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<td>LAT-SS-00152</td>
<td>LAT Tracker Subsystem Specification- Level IV Readout Electronics Requirements</td>
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**CHANGE DESCRIPTION (FROM/TO):**

initial release

**REASON FOR CHANGE:**

**ACTION TAKEN:**

- [ ] Change(s) included in new release
- [ ] DCN attached to document(s), changes to be included in next revision
- [ ] Other (specify):

**DISPOSITION OF HARDWARE (IDENTIFY SERIAL NUMBERS):**

- [x] No hardware affected (record change only)
- [ ] List S/Ns which comply already:
- [ ] List S/Ns to be reworked or scrapped:
- [ ] List S/Ns to be built with this change:
- [ ] List S/Ns to be retested per this change:
- [ ]

**DCN DISTRIBUTION:**

Tracker Subsystem Managers

**SAFETY, COST, SCHEDULE, REQUIREMENTS IMPACT?**

- [ ] YES  
- [x] NO

If yes, CCB approval is required. Enter change request number:

**APPROVALS**

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<th>OTHER APPROVALS (specify):</th>
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<td>ORG. MANAGER: R. Johnson (signature on file)</td>
<td>1/24/03</td>
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<td>Electronics- D. Nelson (signature on file)</td>
<td>1/29/03</td>
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<td>Tracker Engineer- T. Borden (signature on file)</td>
<td>1/10/03</td>
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<td>Design- L. Klaisner (signature on file)</td>
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<td>DCC RELEASE: Natalie Cramar (signature on file)</td>
<td>29-JAN-03</td>
<td>Doc. Control Level: ☐ Subsystem ☐ LAT IPO ☐ GLAST Project</td>
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**FORM # LAT-FS-0012-02**
### LAT Tracker Subsystem Specification–Level-IV Readout Electronics Requirements

**Gamma-ray Large Area Space Telescope (GLAST)**

**Large Area Telescope (LAT)**

**Tracker Subsystem Specification**

**Level-IV**

**Readout Electronics Requirements**

---

**Document Title**

LAT Tracker Subsystem Specification–Level-IV Readout Electronics Requirements

**GLAST LAT SYSTEM SPECIFICATION**

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<td>David Nelson</td>
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**Subsystem/Office**

Tracker Subsystem
CHANGE HISTORY LOG

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<td>2</td>
<td>August 14, 2001</td>
<td>Improved to tie together with the tower testing plan</td>
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<td>August 31, 2001</td>
<td>Tightened the requirement on data noise occupancy</td>
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1 Purpose
This document contains the detailed requirements for the LAT Tracker front-end readout electronics.

2 Scope
The tracker front-end readout electronics encompass all electronics mounted on the tracker module and the cables connecting those modules to the data acquisition in the TEM.

3 Acronyms
GLAST – Gamma-ray Large Area Space Telescope
LAT – Large Area Telescope
TKR – Tracker detector subsystem
TEM – Tower Electronics Module
SSD – Silicon Strip Detector
TMCM – Tracker Multi-Chip Module

4 Applicable Documents
4.1 Requirements Documents

4.2 Electronics Testing and Test Plans
[13] LAT-TD-00333 SEE Test of the LAT Tracker Front-End ASIC
4.3 Conceptual Design Documents


5 Introduction

The Tracker subsystem electronics design is documented in [14], [15], [16], [17], [18], [19], and [20]. This document sets forth the detailed requirements for the Tracker electronics, which flow down from the science requirements set forth in [1] and the top-level Tracker requirements set forth in [3]. The specifications and requirements set forth herein are to be verified according to the plans documented in [7], [9], [10], [11], [12]. In particular, Ref. [12] describes the tests needed for final verification of these electronics requirements for a completed Tracker tower module. Table 1 is a verification matrix that ties the requirements to specific documented tests.

Much of the discussion in this document assumes the basic architecture of the Tracker readout as described in [14]. Each layer of SSDs is connected to a readout module (TMCM) populated with “front-end” amplifier-discriminator chips. Each readout module interfaces the front-end chips to the TEM via “controller” chips and flex cables.

6 Performance

6.1 Trigger Noise versus Efficiency
Noise occupancy for the trigger shall be less than $5 \times 10^{-5}$ within a $0.5 \mu s$ trigger window, with $=99\%$ single-hit MIP efficiency at normal incidence within the detector active area.

6.2 Data-Stream Noise versus Efficiency
Noise occupancy for the data stream shall be less than $1 \times 10^{-4}$ per trigger, with $>99\%$ single-hit MIP efficiency at normal incidence within the detector active area.

6.3 Threshold Uniformity
The RMS variation of the discriminator thresholds across a single front-end chip shall not exceed 10% of the nominal setting.

6.4 Readout Speed and Dead Time
The readout speed and buffering should be sufficient to satisfy the dead-time requirement specified in [3], assuming that the data-stream noise satisfies the requirement 6.2.

7 Signal Processing

7.1 Amplifier Type
The front-end amplifiers shall be charge sensitive with a continuous reset.
7.2 **Shaping Time Constant**
The peaking time of the shaping amplifier shall be 2.0±0.5 µs.

7.3 **Digitization Method**
Digitization shall be done by means of a single threshold.

7.4 **Location of Digitization**
Digitization of the amplifier outputs shall be done within the front-end chip, with no analog signals output from the chip.

7.5 **Threshold Control**
The threshold shall be programmable per chip by an internal DAC, with range at least from 0 to 700 mV, with a resolution of no worse than 6 mV around the nominal operating point (~150 mV).

7.6 **Recovery**
The discriminator output shall stay high no more than 200 µs in the case of charge deposition from a minimum-ionizing fully ionized iron nucleus.

7.7 **Time-Over-Threshold**
Time-over-threshold shall be measured on a per-detector-layer basis, using the Layer-OR trigger-output signal, up to at least 40 µs with no worse than 0.25 µs resolution.

8 **Control**

8.1 **Remote Control**
It shall be possible to configure the electronics by remote commands. This includes all such items as threshold settings and masks.

8.2 **Configuration Read-back**
It shall be possible to verify by non-destructive read-back that the desired bits were in fact written into the chip configuration registers.

8.3 **Control Protocol**
Run-time and calibration control shall be by chip-addressed serial command strings, except for the trigger input for the data latch, which may be a separate serial line, to avoid delay due to collisions.

8.4 **Trigger Protocol**
The trigger-acknowledge signal for latch of the data and the read-event command shall both be accompanied by a trigger identification word of at least 2 bits. These two bits shall be read out with the data stream and checked to ensure that all data from a given events are kept together.

8.5 **Hardware Reset**
There shall be a separate hard reset line that will reset the whole system if pulsed. The reset will guarantee that the system goes into a state in which it is prepared to accept serial command strings.

8.6 **Inputs to the Trigger Logic**
Each tracker layer shall output asynchronously a logical OR of the state of its discriminator outputs (the “Layer-OR” or “Trigger Request”), to be used as input to the trigger logic.
8.7 Trigger Mask
It shall be possible to mask individual channels from the Layer-OR, under external control, independently of the mask for the data stream.

8.8 Trigger Jitter
The timing of the Layer-OR signal leading edge shall vary by no more than ±250 ns for input signals above 2.6 fC.

8.9 Data Mask
It shall be possible to mask individual channels from the data stream, under external control, independently of the mask for the trigger.

8.10 Addressing
It shall be possible to address commands to a specific controller chip or a specific front-end chip.

8.11 Broadcast Address
It shall be possible to address a command in broadcast mode simultaneously to all controller chips or all front-end chips, or to all front-end chips in a single readout module, with the exception of readout of configuration registers or reconfiguration of the front-end chip readout direction.

9 Calibration

9.1 Charge Injection by Command
It shall be possible to inject charge into the amplifiers by serial command with amplitude controlled by an on-chip DAC.

9.2 Charge Injection by External Trigger
It shall be possible to inject charge into the amplifiers by an external differential trigger signal, with amplitude controlled by an on-chip DAC. This need only be implemented for bench tests of the front-end readout chips (to facilitate noise measurements).

9.3 Pulse Height Range and Resolution
The internal calibration system shall have a pulse-height range at least from 0 to 40 fC with a resolution no worse than 0.25 fC.

9.4 Selection of Channels for Calibration
The front-end chip shall include a programmable mask to select any set of individual channels for calibration pulsing.

10 Testing and Monitoring

10.1 Temperature Monitoring
The temperature shall be monitored on at least 8 locations distributed roughly uniformly over the tower height and uniformly on all four sides of the tower.

11 Bias Voltage

11.1 Insulation
All traces, leads, and wire bonds, with the exception of the traces under the detectors on the bias circuit, shall be insulated or encapsulated.
11.2 Isolation of Tower Circuits
It shall be possible during operations to switch on and off the bias supply to any individual side of a tower.

11.3 Isolation of Ladder Circuits
The bias circuit for each ladder shall be separate and isolated from the bus by a resistor of no less than 200 k\(\Omega\) and no more than 500 k\(\Omega\).

12 Power Dissipation
The power dissipated by the Tracker front-end electronics shall not exceed the limit specified in [3].

13 Power, Grounding, and Shielding
Refer to [20] for specification of the Tracker power requirements and to [18] for the grounding and shielding plan.

13.1 Separation of Analog and Digital Grounds
Digital and analog grounds shall be kept separate in the front-end electronics and only tied together, and tied to the shield (the Tracker module mechanical structure), at the point where the cables exit the Tracker. Optional points shall be available to tie the grounds together at front-end electronics module via an SMT resistor.

13.2 Separation of Analog and Digital Supplies
Digital and analog power shall be derived from separate supplies and kept separate everywhere.

13.3 Digital-Analog Coupling
Digital-analog isolation shall be sufficient that digital activity during a readout cycle does not induce above-threshold signals into the amplifiers, assuming the normal operational threshold.

14 Reliability

14.1 Redundancy of Chip Readout Paths in a Layer
Failure of a single amplifier chip shall not result in the loss of data from the other chips in the layer. This is implemented by providing two readout paths for each front-end chip, via the 2 redundant controller chips in each readout module. Each controller chip can change the front-end chip configuration registers to reconfigure the readout.

14.2 Redundancy of Readout Paths from each Layer
Failure of the digital readout of a single layer shall not result in the loss of data from the other layers. This is implemented by providing two parallel sets of readout/power cables and controller chips for each tower side.

14.3 Redundancy in Power Paths
An open failure of a single readout/power cable shall not result in the loss of data. This is implemented by providing two parallel sets of readout/power cables for each tower side.

14.4 Loss of Functionality in the Case of a Power Short
Shorting of power connections in a cable shall not result in the loss of more than \(\frac{1}{4}\) of the layers in a single tower. This is implemented by dividing the readout between four tower sides, each of which shall be on a separate power circuit (separated from the other sides by at least a switch).
14.5 Safety from Power Shorts in a Single Layer
A power short within a layer shall not result in the loss of data from other layers (i.e. each layer shall be separately protected by polysilicon switches).

15 Radiation Tolerance

15.1 Radiation Hardness
Test samples of the tracker readout electronics shall be demonstrated to withstand 10 kRad of ionizing radiation (with the dose accumulated under power and with an active clock) with no loss of functionality and while still satisfying the noise and threshold-matching specifications when connected to complete detector ladders irradiated to the same level.

15.2 Single-Event Latchup Immunity
The CMOS ASICs must be immune to single-event latchup to a level of at least 20 MeV-cm$^2$/mg LET.

15.3 Single-Event Upset Immunity
The configuration registers of the ASICs must be immune to single-event upset to a level such that there is negligible probability of an unintended configuration change during a single run.

16 Cooling
The limitations on temperature of the SSDs are specified in [4].

16.1 Coupling of TMCM to Closeouts
A thermal gasket or adhesive shall lie between the TMCM and the closeout to ensure good thermal coupling in vacuum.

16.2 Current Density in Cables
The current density in the conductors of the cables shall comply with the guidelines in the JPL Handbook D-8208.

16.3 Cooling of Cables
The length of flex cables that passes past the calorimeter shall be clamped securely to the wall of the grid. Within the Tracker the cables shall be clamped securely between the closeouts and tower walls.

17 Mechanical Constraints

17.1 Proximity to Detectors
The front-end electronics readout chips must be mounted within a few mm of the detector strips.

17.2 Minimization of Dead Space
The dead space between tracker towers must be minimized by locating the electronics on the sides of the trays.

17.3 Material in the Bias Circuit
The average number of radiation lengths of material in the bias circuit under the detectors shall be compatible with the tray thickness limits given in [4].

17.4 Material in the Mulit-Chip Module
The average number of radiation lengths of material in the loaded PC board shall not exceed 2%.
17.5 **Modularity of the Electronics Assembly**
The front-end readout electronics for a single tracker layer shall be on a single board that is attached by screws to the tray and removable, if necessary for replacement or repairs, up to the time that the final wire bonds are encapsulated.

17.6 **Encapsulation of TMCMs**
All wire bonds on the front-end electronics board shall be encapsulated with hard epoxy after testing. The boards also shall be conformal coated after testing.

17.7 **Encapsulation of Solder Pins of Connectors**
Connector solder pins on the flex circuits shall be encapsulated with epoxy after soldering and testing.

18 **Interfaces with Other Systems**

18.1 **Communication Protocol**
Communication between the front-end electronics and the DAQ shall be accomplished via serial lines.

18.2 **Trailer Recognition**
Data contents shall never contain a contiguous string of more than 16 zeroes.

18.3 **Data Length**
Data contents in a command or configuration readout shall not exceed 68 bits in length.

18.4 **Multiplexing**
The number of lines going to the DAQ shall be minimized, via simple multiplexing, while still satisfying the redundancy requirements.

18.5 **Signaling**
All digital signals sent onto the circuit board between chips and between the front-end electronics and the DAQ shall be LVDS or pseudo-LVDS. (Here, pseudo-LVDS means low-voltage differential signaling which is not necessarily in compliance with all details of the LVDS standard, such as common-mode range, and not necessarily terminated at the line impedance in the case of short distances.).

19 **Parts**

19.1 **Parts Qualification**
All electronics parts shall be selected and/or qualified in accordance with the mission requirements specified in [5].

19.2 **Layout Rules**
PC board and flex-circuit layout shall be done in compliance with the IPC-2221.

19.3 **Connectors on the TMCMs**
Nano connectors with metal body and captive jackscrews shall be used on the front-end electronics boards.

19.4 **Connectors for the DAQ Interface**
Mil-spec/space-qualified Micro-D connectors with metal body and captive jackscrews shall be used on the DAQ ends of the cables.
## 20 Verification

Table 1 is the verification matrix for the requirements specified herein.

Verification methods:
- T: Test
- I: Inspection
- A: Analysis
- D: Demonstration

Test types:
- F: Functional
- P: Performance
- E: Environmental

**Table 1. Requirements Verification Matrix.**

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