

GLAST Large Area Telescope:

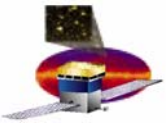
I&T Integration Kickoff Meeting Overview

March 9th, 2004

Pat Hascall
SLAC

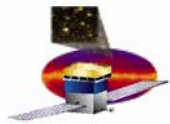
System Engineering Manager

hascallp@slac.stanford.edu
650-926-4266



Topics

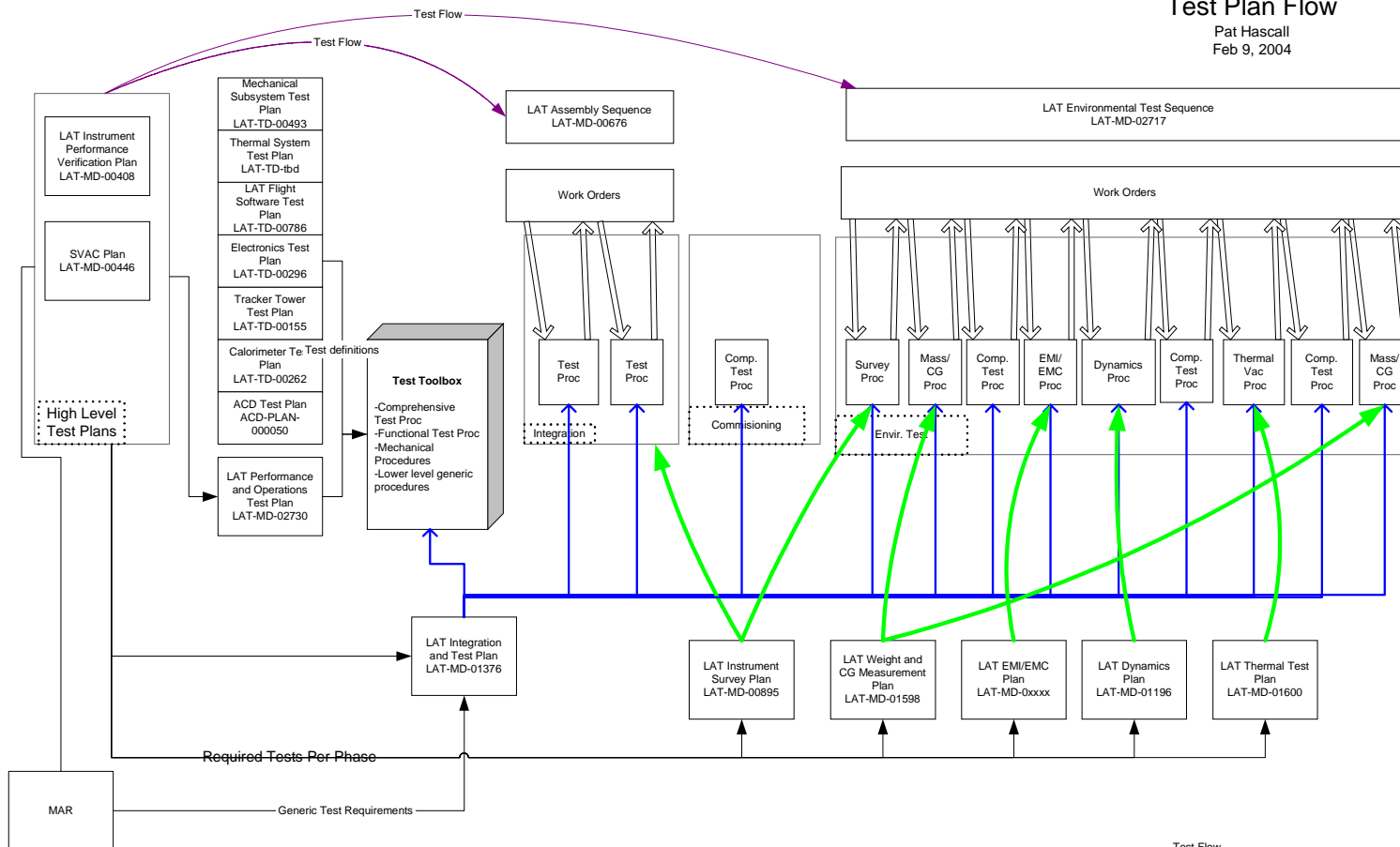
- **Test plan flow**
- **Strategy for completion**
- **Documentation**
- **Schedules**



Test Planning Flow

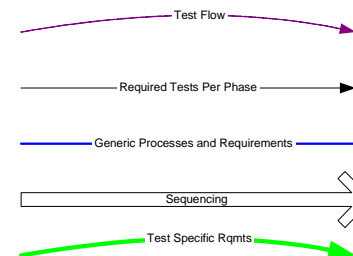
Test Plan Flow

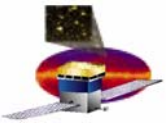
Pat Hascall
Feb 9, 2004



Other notes/issues
 1-Van De Graf test, how and where does it fit
 2-The science cal plan calls for EM tests, not covered under this flow
 3-How does Steve Ritz' data flow verification fit into this plan?
 4-Where are algorithms for EGSE software (and SAS software) specified? They need to be consistent

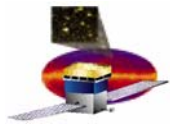
Other plans/procedures that are valuable resources:
 LAT Integration and Test Subsystem Electrical Performance Test Plan (Wai-LAT-MD-01055)
 GLAST LAT I&T Testing Requirements Document - (Claus - LAT-TD-02834)
 LAT SVAC Test Requirements Plan (Eduardo, LAT-MD-01587)



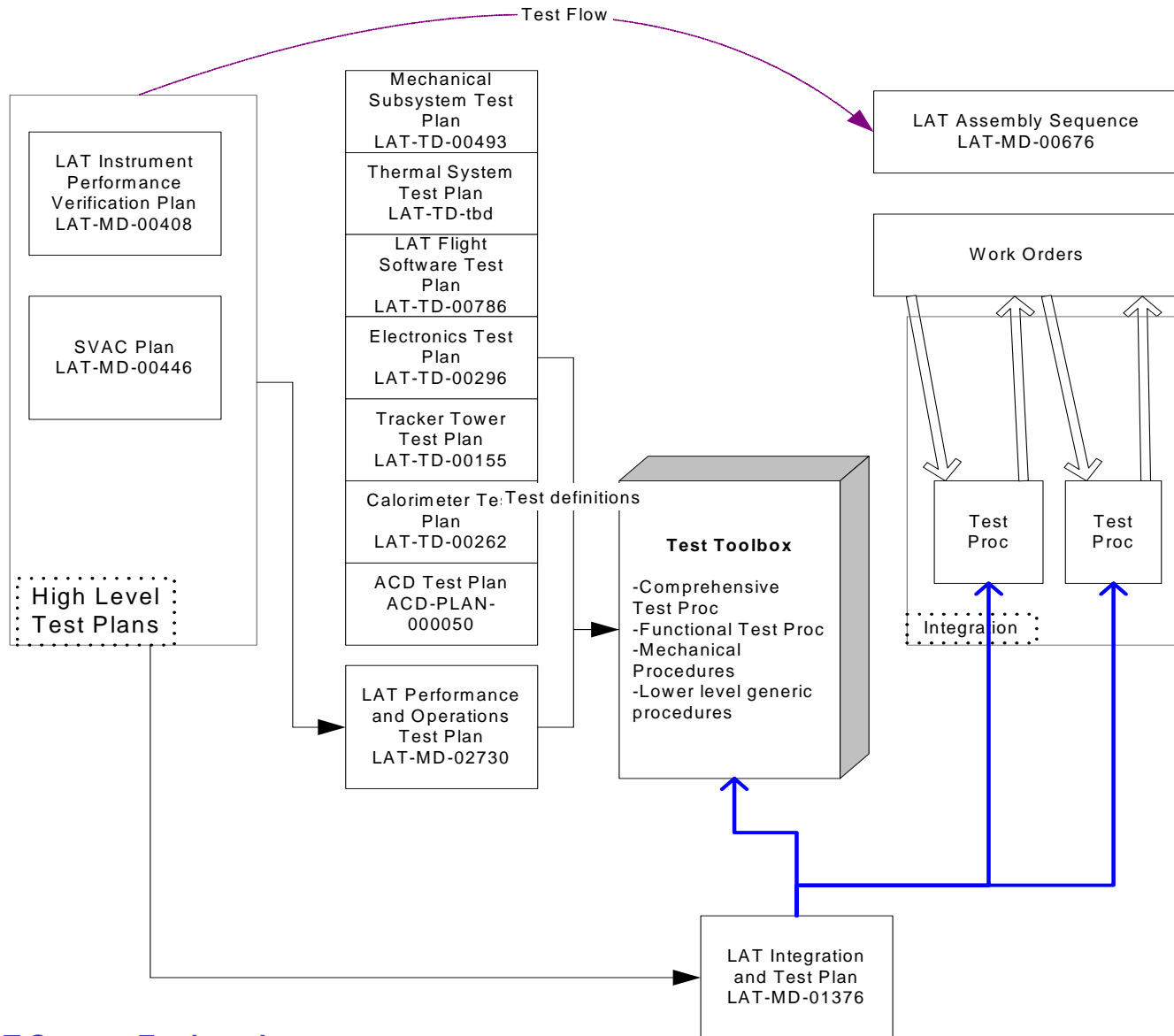


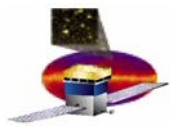
Strategy for Completion

- **Phased approach to provide planning necessary for first 6 months of integration**
- **Focus is on Calorimeter and Tracker first, followed by DAQ boxes, then ACD**



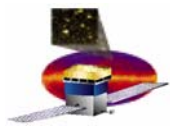
Near Term Test Planning Flow





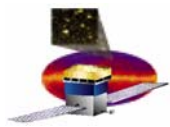
LAT Assembly Sequence

- **LAT Assembly Sequence LAT-MD-00676**
 - **Contents**
 - **Defines in detail the sequence of operations necessary to integrate the LAT**
 - **Focuses on mechanical operations, and calls out electrical tests to be run from separate procedures**
 - **Status**
 - **Draft completed, some refinement needed**
 - **Schedule**
 - **Personnel reprioritized, ETC TBD**
 - **Mitigation**
 - **Sufficient detail available to proceed, remaining work is primarily clean up**



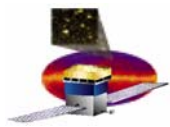
LAT Performance and Operations Test Plan

- **LAT Performance and Operations Test Plan LAT-MD-02730**
 - **Contents**
 - Defines at a high level each of the individual tests (e.g. TE103, Tracker Bias Current)
 - Define when the test will be run (Functional Test, Comprehensive Test, Integration test ...)
 - **Status**
 - Draft initiated (samples on next viewgraphs)
 - Details worked in weekly meetings with I&T and subsystems
 - Will include definition of 2 tower test derived from End-to-End Committee results
 - **Schedule**
 - First cut out by end of month as part of an incremental release series
 - **Mitigation**
 - Information generated by a team effort (including members of End-to-End Committee), so test development can proceed in parallel



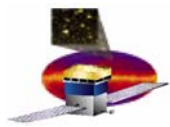
Test Definition Sample

- **Tracker GTRC configuration register and readback**
 - The GTRC chips are sequentially addressed and their configuration registers loaded with a bit pattern. Each time the register is read back and checked for errors. The test is repeated with the complement of the bit pattern. The test then is repeated with a broadcast address for writing the register, followed by sequential readback. (Based on Tracker Test TE201)
- **FSW Tracker Configuration Test**
 - This test shall verify the ability of the SIU to configure the TKR subsystem as desired and read back the necessary configuration information to completely determine the TKR subsystem configuration (Based on FSW test 7b)



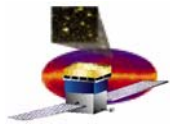
Test Instance Format Sample

ID	Test	Incoming	Tower	Two Tower	...	Comp.
	Power Consumption	X	X			X
	Temperature	X	X			X
	Leakage Current	X	X	X		
	GTRC configuration	X	X	X		
	GFTE left/right configuration	X	X	X		
	GFTE split configuration	X	X	X		
	Reset	X	X			
	Threshold Scan	X	X	X		X
	Charge Injection Scan	X				
	Gain and Noise	X	X	X		X
	Layer Timing	X	X	X		X
	Occupancy	X	X	X		X
	Occupancy w/readout	X	X	X		X
	Muon Scan	X	X			
	High Rate/ Deadtime	X	X	X		X
	...					
	Combined Charge Injection Scan		X	X		
	...					
	FSW Tracker Configuration Test					X



Integration Drawings

- **Integration Drawings**
 - **Contents**
 - Defines how the pieces delivered to I&T relate and provides some assembly information
 - In some cases, provide a model with internal details removed to facilitate model usage (outline drawings)
 - **Status**
 - Drawing tree defined
 - Model and drawing completion on hold
 - **Schedule**
 - Will take approximately 2 months after effort is restarted to complete model integration and drawings
 - **Mitigation**
 - Many of the models can be used now to get views necessary for integration procedures



Drawing Tree

LAT Level Drawing Tree

Rev 5
Jan 15, 2004

Pat Hascall

