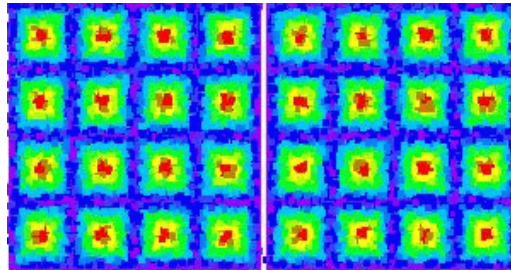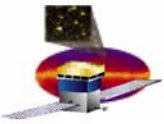# TKR Detector and Front-end Electronics


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Instrument Analysis Workshop 1

SLAC, June 8, 2004

Outline

- ❑ Overviews of TKR tower
- ❑ Overview of a single tray
- ❑ Overview of TKR front-end electronics
- ❑ Profile of one-channel analog signal
- ❑ Readout sequence of strip data
- ❑ Control parameters (registers)
- ❑ Calibration: gain and noise
- ❑ Calibration: threshold
- ❑ Calibration: TOT
- ❑ Gotchas (limitation and exceptional case)
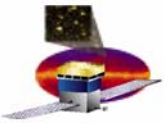
Overview of TKR Tower
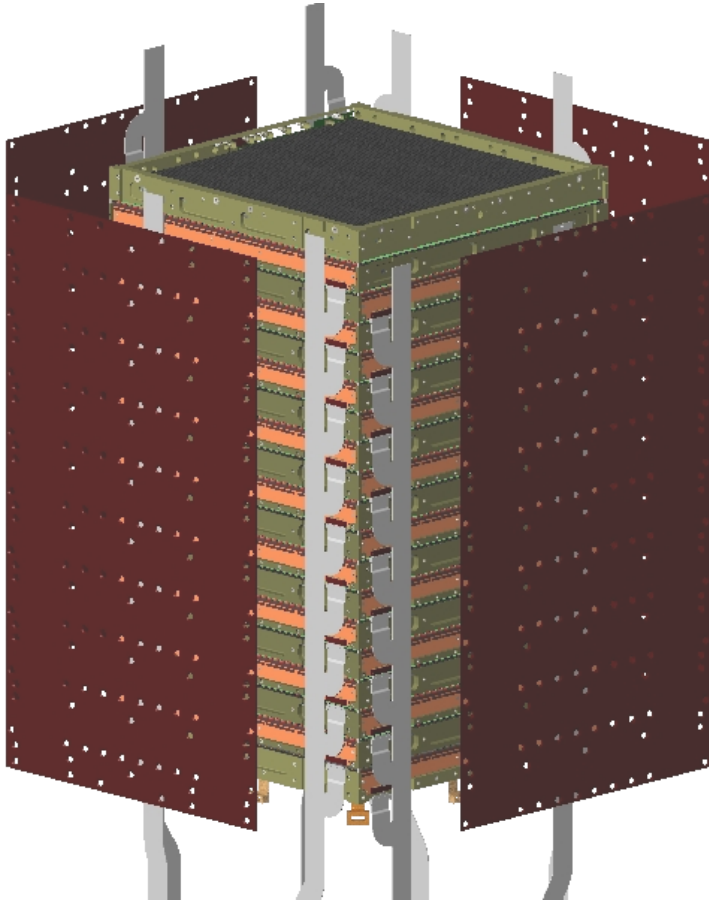
Oviewview of one tower TKR

16 tungsten layers

36 silicon-strip detector layers
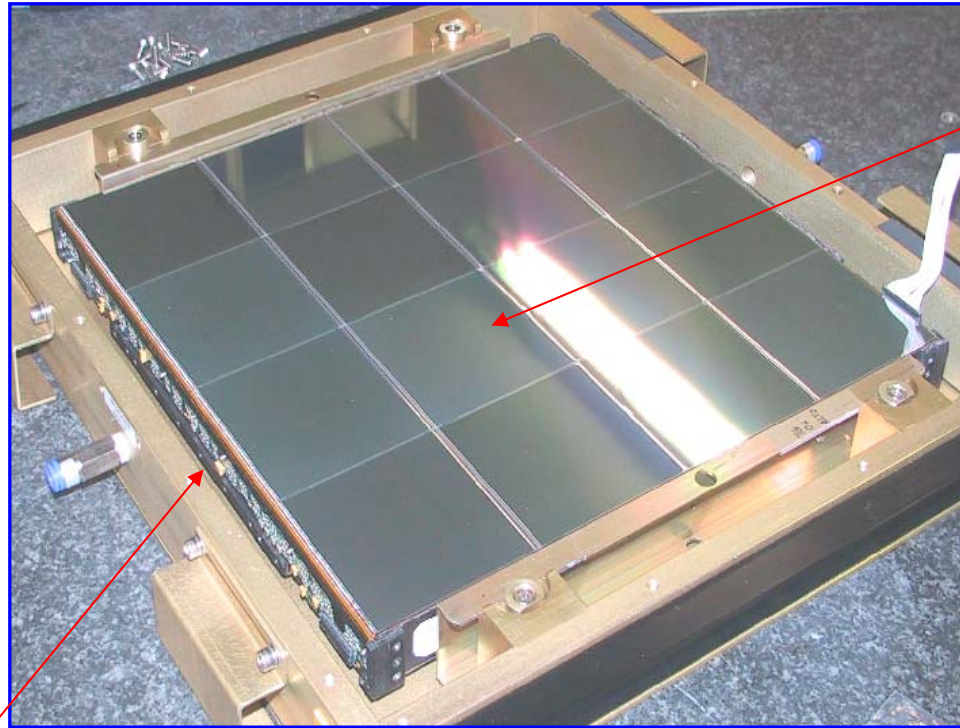
Strip pitch = 228 μm

1536 chanels per layer

-> 36*1536 = 55,926 channels / tower

~110,000 channels for two towers

1 tungsten layer + 2 (x,y) SSD layer

-> 'Tray'

Overview of a Single Tray

2 Silicon-Strip Detector layer (x,y) + Converter (tungsten)

2 mm gap between x,y SSD layers

Tracker Front-end electronics module (TMCM)

8.95x8.95 cm^2/SSD *16 = ~ 36x36 cm^2

TKR Front-end Electronics Modules (TMCM)

GTFE (Front-End) ASICs: 24
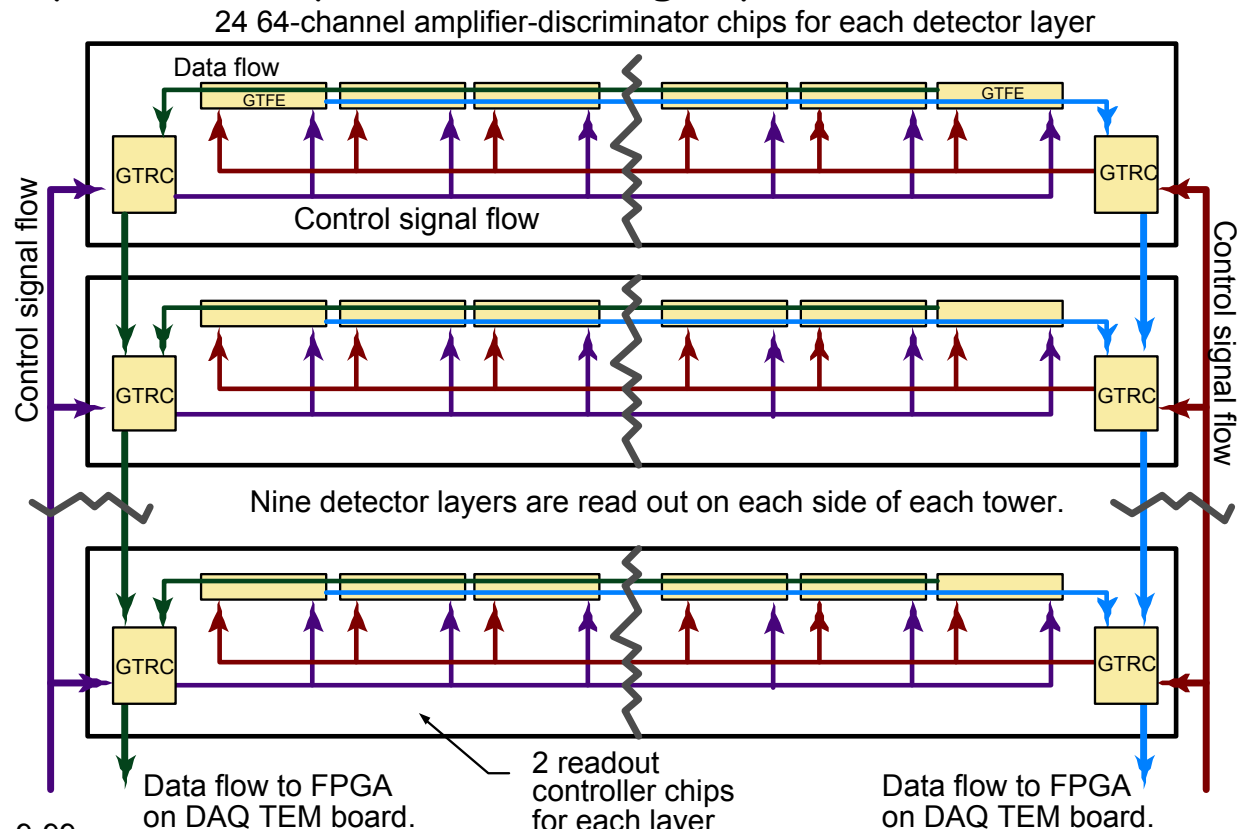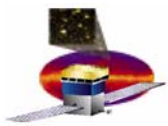64 channels/chip * 24 = 1536 channels/layer

Pitch adapter

GTRC (Read-out Controller) ASICs: 2
(This is where the TOT is calculated.)
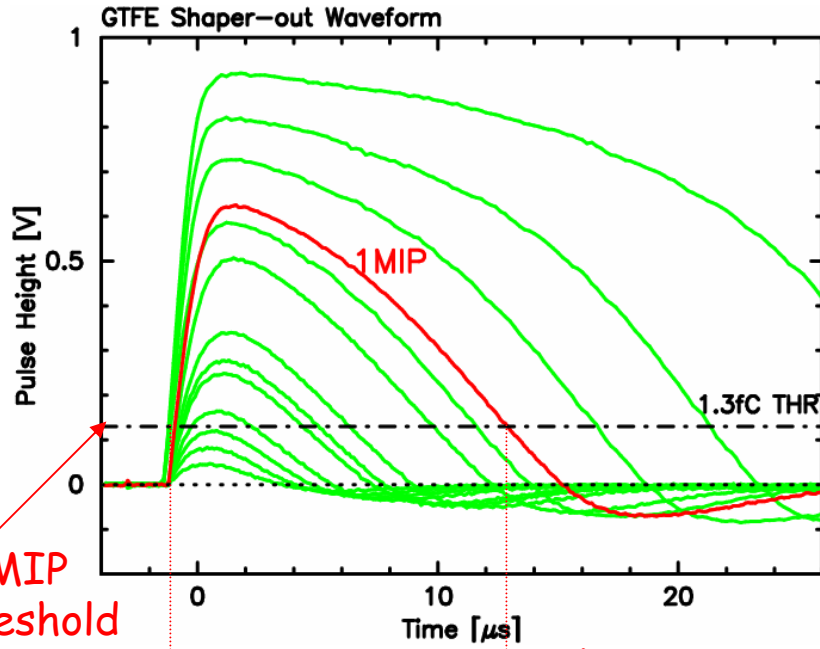
Overview of Readout Electronics

❑ Based on 2 ASICs

  ▪ 64-channel amplifier-discriminator chip (GTFE); 24 per module.

  ▪ Readout controller chip (GTRC); 2 per module.

❑ Two redundant readout and control paths for each GTFE chip ("left" or "right") makes the system nearly immune to single-point failures.

❑ **Programmable** channel **masks** and **threshold** DACs.

❑ Internal, programmable **charge-injection** system.

❑ **Trigger** implemented from **OR of all channels/layer.**

24 64-channel amplifier-discriminator chips for each detector layer

Data flow

GTFE

GTRC

Control signal flow

Control signal flow

Nine detector layers are read out on each side of each tower.

GTRC

GTRC

Control signal flow

2 readout controller chips for each layer

Data flow to FPGA on DAQ TEM board.

Data flow to FPGA on DAQ TEM board.

Profile of One-channel Analog Signal on GTFE

GTFE Shaper—out Waveform

1MIP
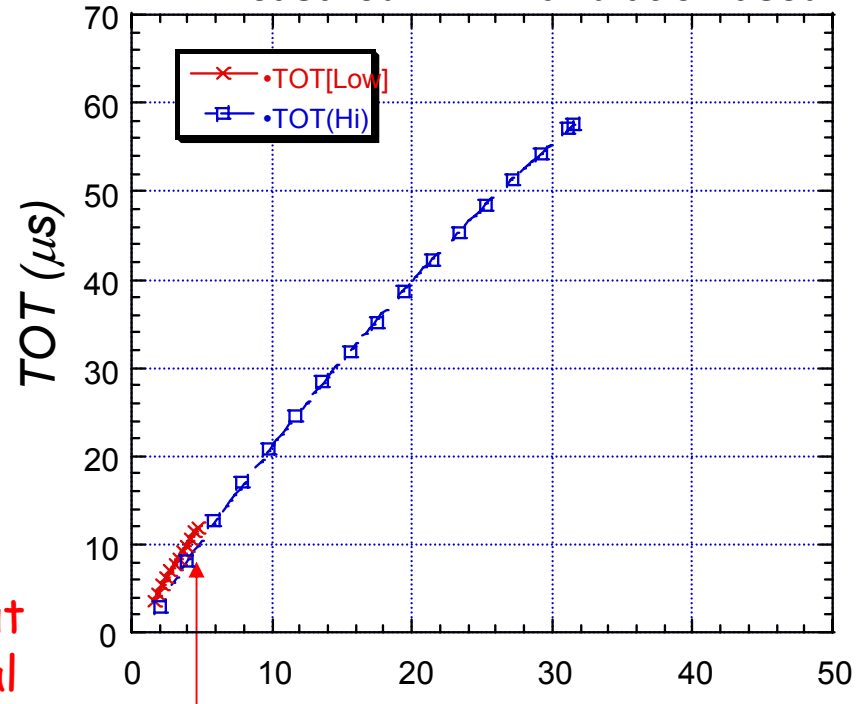
1.3fC THR

1/4MIP Threshold

Comparator-out ->Trigger signal (TRIG)

TACK delay

Time over threshold (TOT)

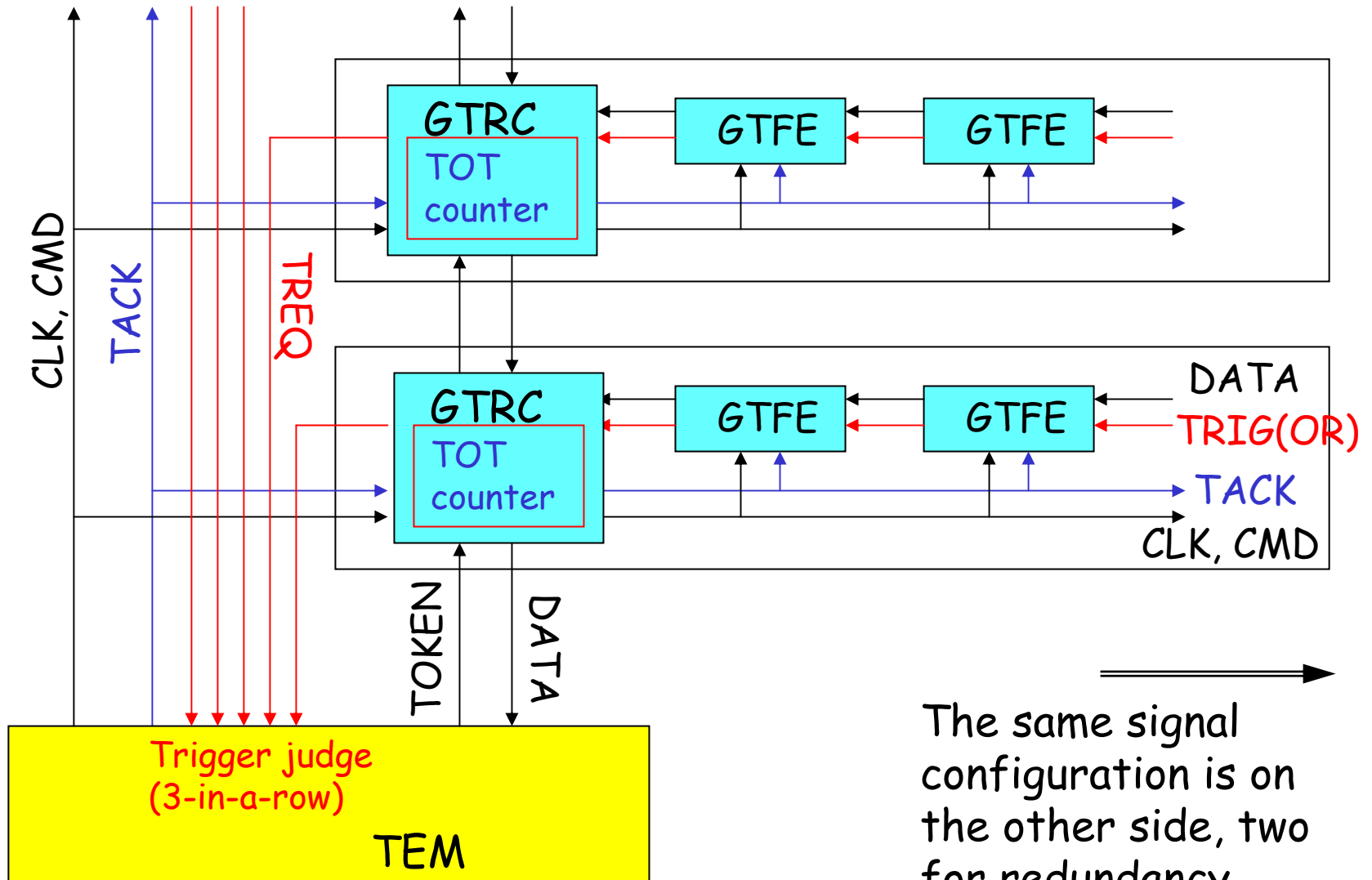Trigger acknowledge (TACK)

TOT vs Input Charge
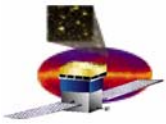Measured DAC Calibration used

•TOT[Low]
•TOT(Hi)

1MIP (~5fC)

can be calibrated
with range 0(LOW), 0-1 MIP
        range 1(HIGH), 0-8MIP
in the internal calibration system

Detail Schematic of Readout Signals (one side)

CLK, CMD

TACK

TREQ

GTRC
TOT counter

GTFE   GTFE

GTRC
TOT counter

GTFE   GTFE

DATA
TRIG(OR)
TACK
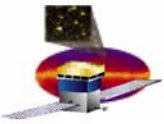CLK, CMD

TOKEN   DATA

Trigger judge (3-in-a-row)

TEM

The same signal configuration is on the other side, two for redundancy.
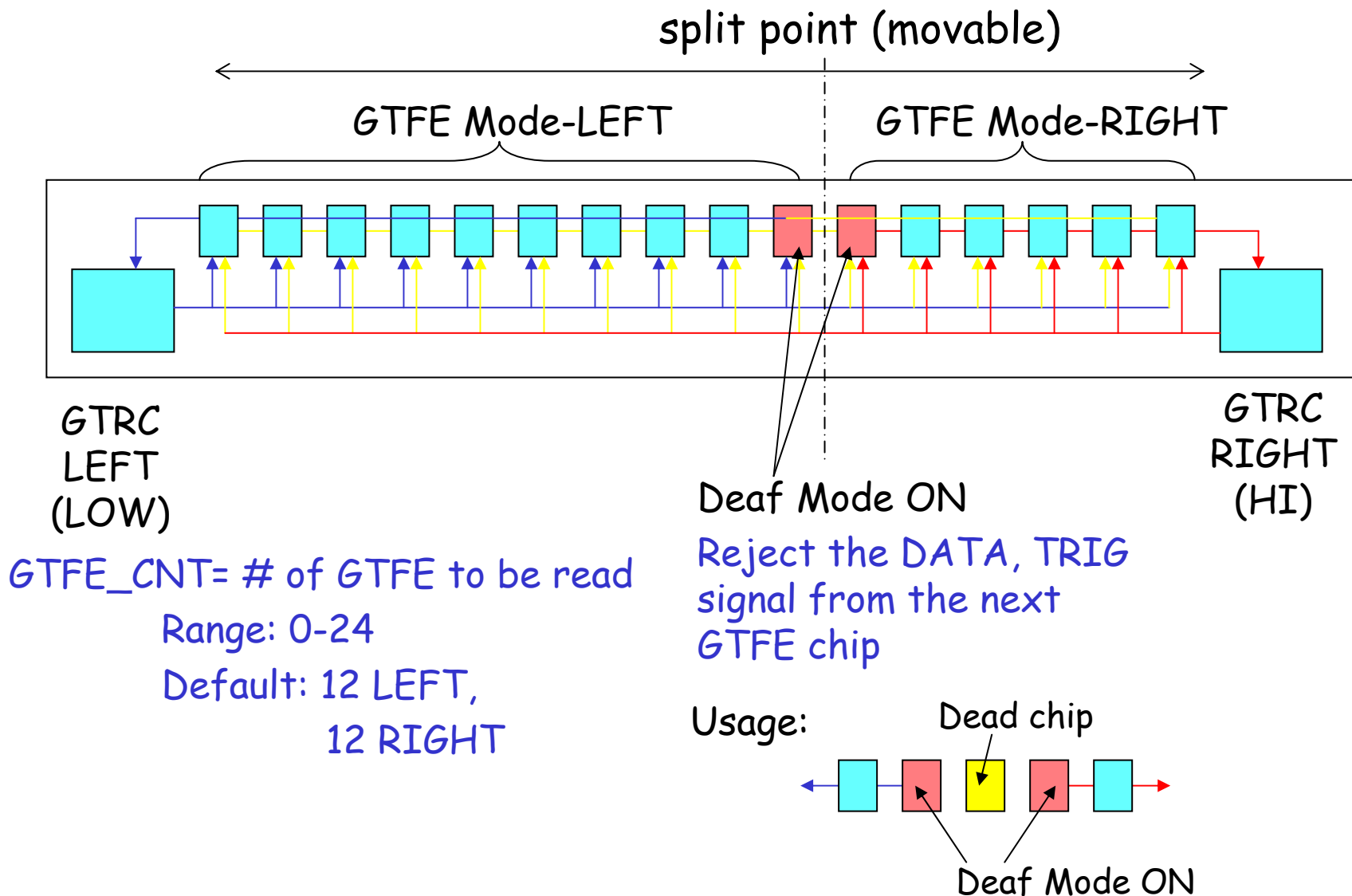
Readout Sequence of Strip Data

1. If a shaper-out signal of a channel in a GTFE chip is over the threshold, TREQ signal is issued and transferred to TEM.

2. TEM check trigger status. If a trigger condition (3-in-a-row?) is satisfied, TEM send TACK signal to all layers and latch hit strip data into GTFE event buffer.

   - TACK signal also start TOT counter in GTRC. (Notice! Not TREQ)
   - GTFE has 4 event buffers.

3. TEM send READ-OUT command and transfer event data from GTFE to GTRC event buffer.

   - GTRC event buffer is limited to 64 hit-strip.   Max: 64x2=128
   - GTRC has 4 event buffers.   strips/layer

4. TEM send TOKEN signal and transfer event data from GTRC to TEM one-by-one layer.

   - GTRC wait to send data until the process of READ-OUT command finish and TOT counter terminate. TOT counter saturates at 1000 clock cycles (=50μs). In a case that TOT counter overflow, GTRC start to send data at the overflow point, 1000.

Control Parameters (Registers)
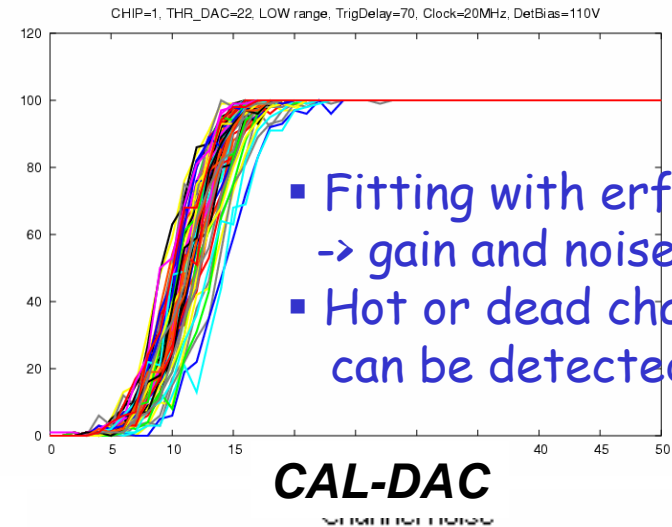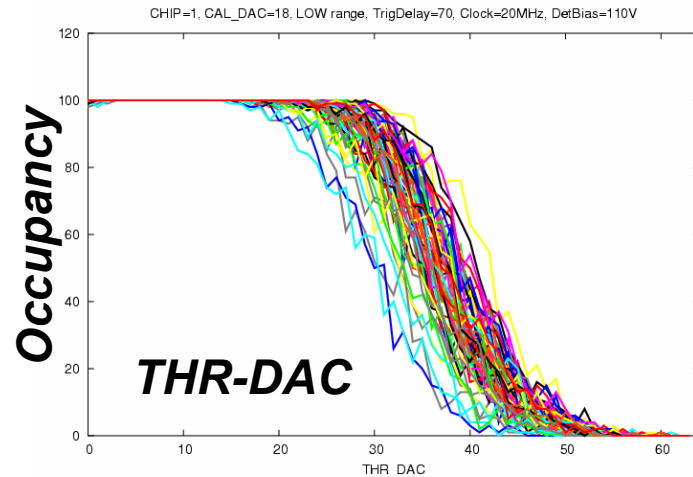
- ❑ GTFE (c.f. LAT-SS-00169)
  - ▪ MODE registers: 2bit
    - Select LEFT or RIGHT mode
    - Deaf mode ON/OFF
  - ▪ DAC registers: 7bit+7bit
    - THR_DAC:
      - set threshold level of comparator.
      - **(0-2 MIPs)**
      - range: ~ 0.05-10 fC
    - CAL_DAC:
      - set pulse height of calibration strobe signal.
      - **(0-8 MIPs)**
      - range: ~ 0.072-43 fC
  - ▪ MASK registers: 64bit
    - • channel mask
    - • trigger mask
    - • calibration mask

- ❑ GTRC (c.f. LAT-SS-00170)
  - ▪ GTFE_CNT
    - Number of GTFEs to read.
    - Define the split point of LEFT and RIGHT
    - Range: 0—24
    - Default: 12 for both LEFT and RIGHT
  - ▪ SIZE
    - Max number of hits to get from GTFEs
    - 0-64, default: 64
    - **Max hits/layer: 128 hits** can be read using both LEFT and RIGHT sides.
  - ▪ TOT_EN
    - 0: Disable TOT
    - 1: Enable TOT (default)
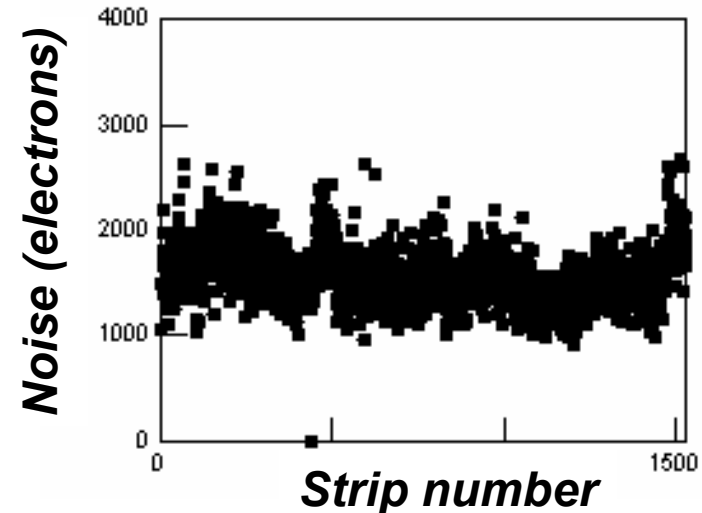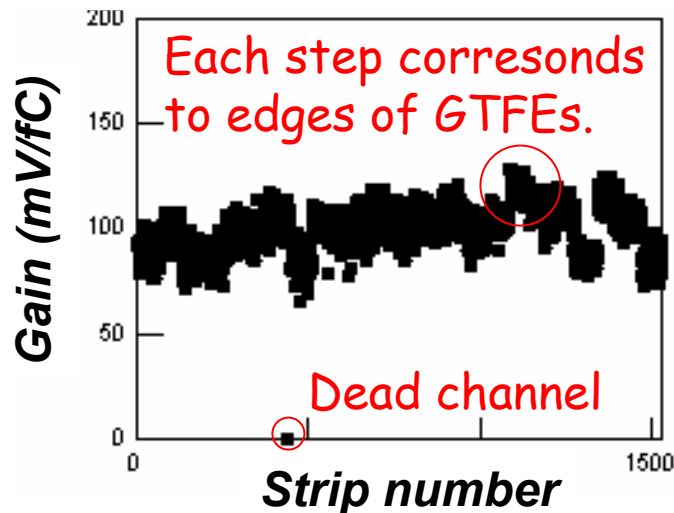
Control parameters (LEFT RIGHT)

split point (movable)

GTFE Mode-LEFT   GTFE Mode-RIGHT

GTRC
LEFT
(LOW)

GTRC
RIGHT
(HI)

Deaf Mode ON

Reject the DATA, TRIG
signal from the next
GTFE chip

GTFE_CNT= # of GTFE to be read

Range: 0-24

Default: 12 LEFT,

12 RIGHT

Usage: Dead chip

Deaf Mode ON

Calibration: Gain and Noise

❑ Threshold scan and charge-injection scan

CHIP=1, CAL_DAC=18, LOW range, TrigDelay=70, Clock=20MHz, DetBias=110V

CHIP=1, THR_DAC=22, LOW range, TrigDelay=70, Clock=20MHz, DetBias=110V

Occupancy

THR-DAC

THR DAC

- Fitting with erfc or erf -> gain and noise
- Hot or dead channels can be detected.

CAL-DAC

❑ Gain and noise distribution

Gain (mV/fC)

Each step corresonds to edges of GTFEs.

Dead channel

Strip number

Noise (electrons)

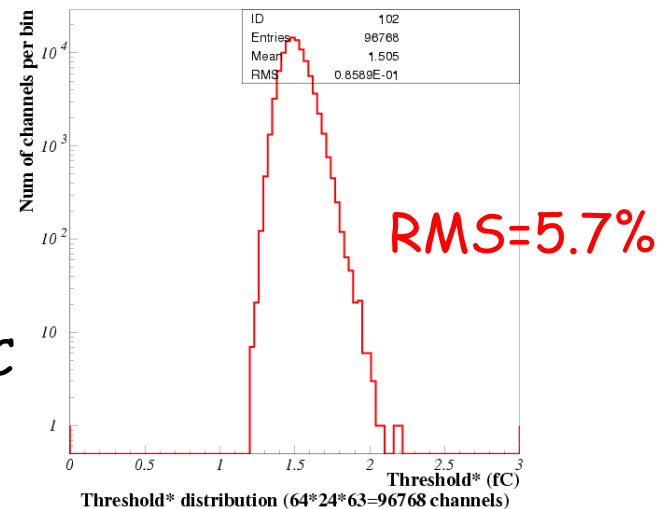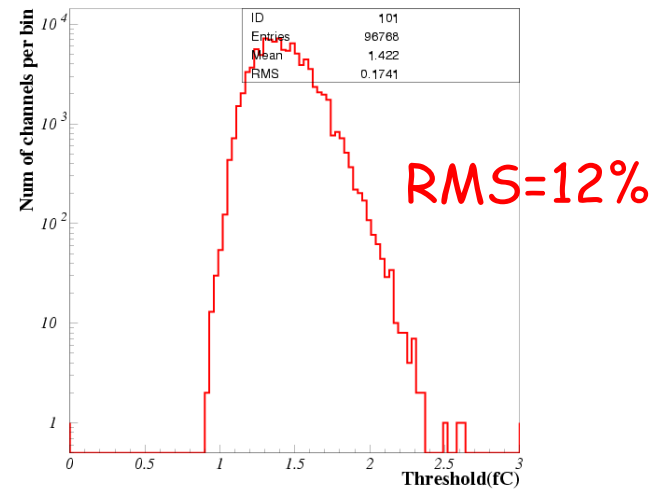*Strip number*

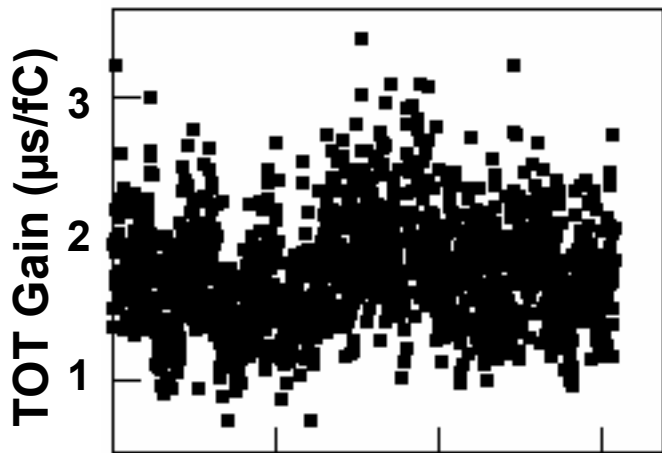# Calibration: Threshold Level

GTFE
Channel-to-channel
gain variation
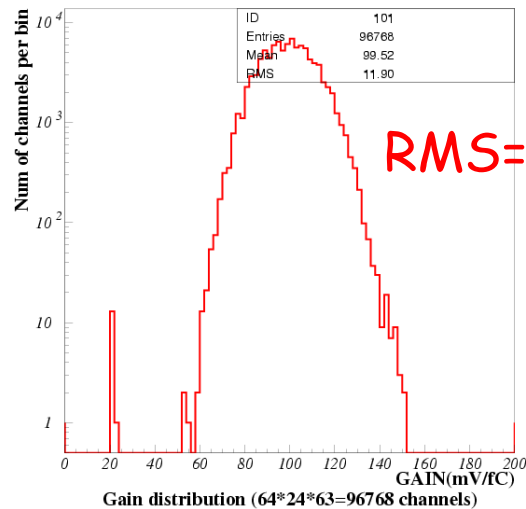
Threshold variation in a single
nominal THR-DAC setting (30L).

RMS=12%

RMS=12%

RMS=5.7%

Threshold variation in a THR-DAC
setting, correcting gain variation
for each GTFE.
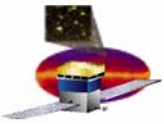
Calibration: TOT

□ TOT gain (μs/fC) variation is expected to be fairly large.

Strip #

□ How to calibrate TOT gain (Hiro).

- Perform charge-injection scan for all channels and obtain channel-to-channel variation of TOT gain (μs/CAL-DAC).

- Take data of TOT for cosmic-ray muons and investigate the distribution per GTFE. The peak would corresponds to 1 MIP (5 fC).

- Compare the TOTs for calibration strobe signal in the charge-injection scan and for cosmic-ray muons, and calibrate the scale of (CAL-DAC) and (fC).
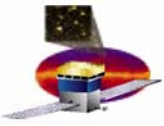
Trigger Occupancy

Noise trigger rate in nominal threshold

~3 Hz/GTFE = ~0.5 Hz/channel

Duration of the noise trigger

~ shape time = 2 μs (c.f. 1MIP = 10μs)
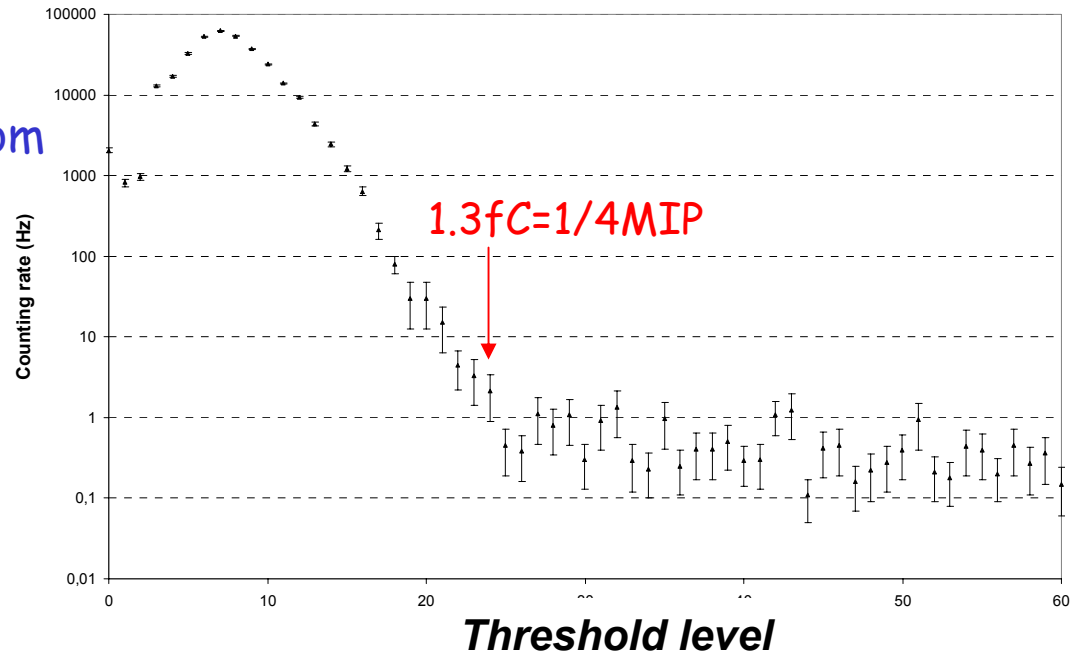
Occupancy/strip

0.5 Hz * 2 μs = 10^{-6}

Trigger rate of 64 channels of one GTFE chip in EM mini tower

This estimation agrees with the result of random trigger test in EM mini tower (by Pisa group).

Noisy channels can be disabled with trigger mask register. (data of the channel is still available.)

1.3fC=1/4MIP

Counting rate (Hz)

Threshold level

Gotchas (limitation and exceptional case)

❑ Limit of TOT counter

- TOT counter saturate at 1000 count. It corresponds to 50 μs. (c.f. 1 MIP ~ 10 μs.)

❑ Limitation of calibration-strobe signal in GTFE

- Calibration strobe signal of GTFE used in charge-injection tests is a signal with a duration of 512 clock cycles = 25.6 μs. Thus, we cannot simulate TRIG signal longer than 25.6 μs with the internal calibration system.

❑ Too late TACK in a small signal

- Small signal events with the pulse height very close to threshold will be missed at the TACK time, which cause the event with trigger but no hit. The probability of such events was 10^{-5} in EM tower (Eduardo).

❑ 2 TACK in one TREQ signal

- In a case that multiple TACK are sent within one long trigger signal, TOT in the second readout event shows an illegal number (2044).