GLAST Large Area Telescope:

SVAC Workshop
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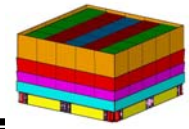
AntiCoincidence Detector (ACD) Subsystem Performance Calibration and Verification

Alex Moiseev
Robert Hartman
David Thompson

NASA Goddard Space Flight Center
With contributions from Luis Reyes, Eric Charles, Larry Wai, and others

ACD Pre-Shipping Tests



ACD System-level Tests of numerous configurations have been performed during and after ACD integration at Goddard from the mid-May to August 2006

The idea of the tests during integration was to perform the tests after every major step in the integration in order to eliminate the need to do some disassembling in the case of discovering the problems later.

Current ACD Full Functional test contains TrigOps to test ACD Performance; in the earlier stages we run parts of tests to save the time

ACD Performance test – test of ACD capability to detect charged particles; subject of this test is to determine mip peak positions and pedestals for every ACD channel. For the ribbons it is a light yield along the ribbon length

ACD Testing software was still in development stage during ACD tests at Goddard, which created additional problems

ACD Pre-Shipping Tests (cont.)

"Partial" performance tests during ACD integration:

1. Light tightness tests – performed after every tile/ribbon row installed

Purpose of this test is to ensure that there is no light leak in installed parts. If High Voltage (HV) is applied, light leak can severely damage the PMT. Light leak can be:

– in the tile light-tight wrapping (made of black tedlar), especially at the tile edges where tedlar can crack

– in the tile fiber connector area where the irregular shape connector is wrapped

– in the fiber cable Sumitube black tubing – possible pin-holes; also in tubing-to-optical connector joining points

– in the area of fiber cable coupling to the PMT housing – most often occurs

– around tile mounting holes

The sequence of this test:

– cover whole ACD by light tight tent; run "Rate Monitor" script to get every channel "normal" rate at nominal HV

– open the tent; run "Rate Monitor" script with HV 300 V less than nominal. Get rates. If none of the channel rate exceeds "normal" rate by more than 10%, raise HV by 100 V and repeat the test

– if some excessive rate is found, locate light leak by covering parts of failing channel and using "pencil" light source to detect the leak place

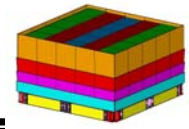
– test is completed and ACD is ready for further integration, if all rates with open tent are within 10% of the normal rate

ACD Pre-Shipping Tests – Partial Performance tests

2. Particle detection capability – performed several times during the integration to check that mip peak positions are in reasonable places in corresponding PHA histograms

3. High Voltage selection – performed after all tiles installed to select the value of operating HV. Every FREE board (up to 18 PMT) has its own HVBS, and the idea is to select optimal HV when the "weakest" channel has a mip peak separated from pedestal by approximately 400 ADC counts. This provides us necessary VETO threshold precision setting and desired range of signals in "Low range" – ideally to 6-8 *mip*s. In spite of careful PMT assignment to FREE board to reduce the range of mip peak position variation across FREE (R. Hartman), there are still some channels peaking at ~800 ADC counts. This reduces the range of signals in "Low range", but has no affect on ACD efficiency
HV values vary from board to board from 720V to 840V.

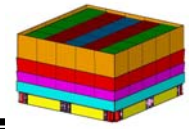
Selected HV Values



These HV are recommended for ACD operation; all calibrations are made with these HV values; change of any of them would require full ACD recalibration

FREE card	GARC number	Chosen HV, Volts	Range of tile *mip* peak positions, except ribbons (pedestals subtracted)	Limit of *mip* signals in PHA Low Range, in *mips*
1L	0	740	400-800	0 – (3.5 – 7)
1R	1	760	400-800	0 – (3.5 – 7)
2LA	2	720	400-650	0 – (4.5 – 7)
2LB	3	730	400-700	0 – (4 – 7)
2RA	4	715	400-650	0 – (4.5 – 7)
2RB	5	745	400-800	0 – (3.5 – 7)
3L	6	820	400-800	0 – (3.5 – 7)
3R	7	800	400-800	0 – (3.5 – 7)
4LA	8	755	400-700	0 – (4 – 7)
4LB	9	740	400-700	0 – (4 – 7)
4RA	10	760	400-850	0 – (3 – 7)
4RB	11	745	400-900	0 – (3 – 7)

Full Functional Test



- ***A successful Full Functional Test of the fully integrated flight ACD was performed before and after vibration/acoustics and at four temperatures: +35 C, +23 C, 0 C, and -25 C.***
- ***Document numbers are ACD-PROC-000270 (functional/performance) and ACD-PROC-000352 (margin).***
- ***The test covers all aspects of the ACD functional areas such as***
  - ***Voltages, currents, temperatures***
  - ***Commanding***
  - ***Electronics performance***
  - ***Detector operation***
  - ***Margin testing (varying electronics voltages and clock frequencies)***

Full Functional Test – *Basic Power On Notes*

- ***Voltages – 28 V and 3.3 V supplied by the GASU. The flight GASU may be supplying slightly lower voltages than the engineering GASU. It is important to re-test the ACD with only one set of LVDS drivers enabled (default power-on mode is both sets on). High Voltage (0-1250 V) generated within the ACD.***
- ***Currents – measured by the GASU. The ACD power cannot be measured directly, because the DC-DC converters in the GASU consume some power.***
- ***Commanding – checks that all registers can be written and read, including broadcast commands; checks parity error detection***
- ***Electronics Setup***
  - ***Check settings for maximum number of PHA values per GARC***
  - ***Check enable/disable settings for each PHA channel***
  - ***Verify setting of PHA threshold (zero-suppress threshold)***
  - ***Check (but not change) bias for 3.3 V line on each GARC***
  - ***Check electronics noise level in GAFE (analog ASIC)***

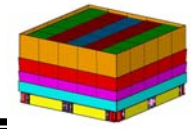
Full Functional Test – *Timing/TCI Tests*

- ***Hold Delay – optimize time that the PHA signal is held before sampling***
- ***Hitmap Delay – test operating range for delays in the Hitmap discriminator to match the TACK arrival time***
- ***Hitmap Timing – check Hitmap Delay settings at different widths of Hitmap discriminator***
- ***Test Charge Injection (TCI) with notes about some anomalies observed:***
  - ***VETO threshold – excess counts seen on one channel at cold temperatures***
  - ***High Level Discriminator threshold – one channel shows unexpected counts***
  - ***PHA Regular Range (low and high sections) – nonlinearity increased (although not badly) when ACD was integrated onto the LAT***
  - ***PHA High Range (low and high sections) – high section is quite nonlinear, but not a problem.***
  - ***Hardware Counters***

Unexpected Counts Testing Anomaly PR ACD-02334-009

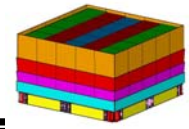
- ***During each of the cold cycles during the thermal vacuum test, we observed 2-4 excess counts on one electronics channel of the ACD during a test.***
- ***The test was done using charge injection and was a test of a high VETO threshold (5 strobes; should have recorded no counts).***
- ***Either the VETO threshold was not set properly, or the test charge was larger than expected.***
- ***The excess counts appeared on the last GAFE of the last GARC, suggesting a possible end-of-test-cycle clearing error, possibly due to timing, but we have no way to confirm this suspicion.***
- ***It is also possible that we have a channel with an instability, because this same error was seen on this channel in chassis cold tests.***
- ***The operational performance of this channel is excellent at all temperatures.***
- ***If we found excess VETO rate in orbit, we could re-set the threshold. It has very wide dynamic range.***

High Rate Testing Anomaly PR ACD-02334-016



- ***During two of the four transitions from hot to cold during the thermal vacuum test, we observed high rates (up to 5 KHz) on one tile detector of the ACD. Temperature was between 10 C and –15 C.***
- ***The high rate in both cases settled down to a normal rate (< 100 Hz) by the time temperature stability was achieved.***
- ***The test script that was running collected only rate data, so we have no other information about the output from that tile. We do not even know which of the two phototube signals might have given the high rate, because the hardware counters sum the signals.***
- ***This channel (both phototubes) produces good data in every functional test we have done, including a run at 0 C.***
- ***Because it is a transient problem, not even seen in every transition, we have been unable to diagnose this problem. Generally noise decreases with lower temperature. It was not seen in chassis tests.***
- ***If a high rate on a channel appeared in orbit, we have the option of disabling a phototube signal. Loss of one signal would be acceptable for ACD performance.***

ACD Monitored Parameters



Monitored Parameter Family	Parameter Name
Bias DAC	LE and HE Bias Slope, Offset and Preferred Setting
GAFE Noise	Vernier sharpness; Noise Threshold
Veto Step (AcdVetoCal)	Veto slope; Veto offset
HLD Step	HLD slope; HLD offset
Low (Regular) Range PHA linearity calibration	Low_slope;Low_offset;Low_MSE;High_slope;High_offset;High_MSEAuto_LE_mean; Auto_LE_step; Auto_HE_mean
High Range PHA linearity calibration	Low_slope; Low_offset; Low_MSE; High_slope; High_offset; High_MSE
Pedestal (script)	Mean value; Distribution Width
AcdHitMap Delay	Channel Hit Map delay; Hitmap Delay mean; HitMap delay SD; HitMap Delay optimal
ACd Hold Delay	Channel Hold Delay; HoldDelay optimum; HoldDelay StDev
HVBS	HV intercept; HV slope; HV Current
FREE	FREE currentVoltage Temperature
Histograms	MIP peak position; MIP peak width; Pedestal position
Rates	Hardware rates; Software rates

Now moving to Performance tests 

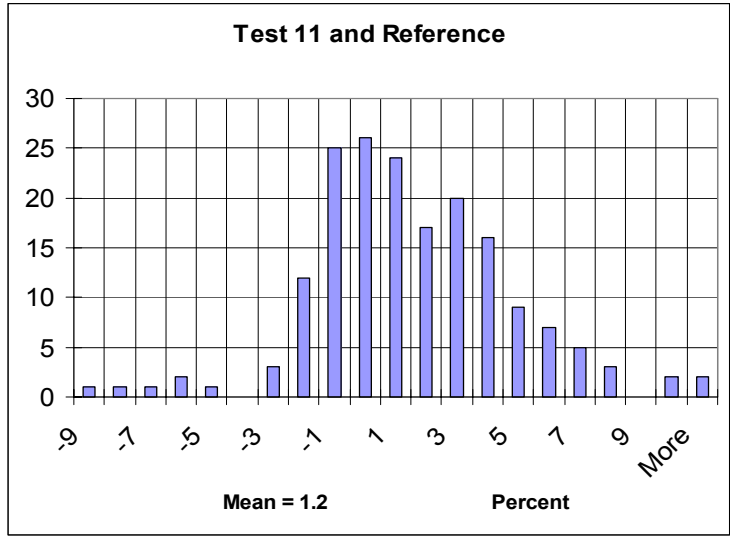
ACD Performance tests at Goddard

List of Performance tests at Goddard, summer 2005

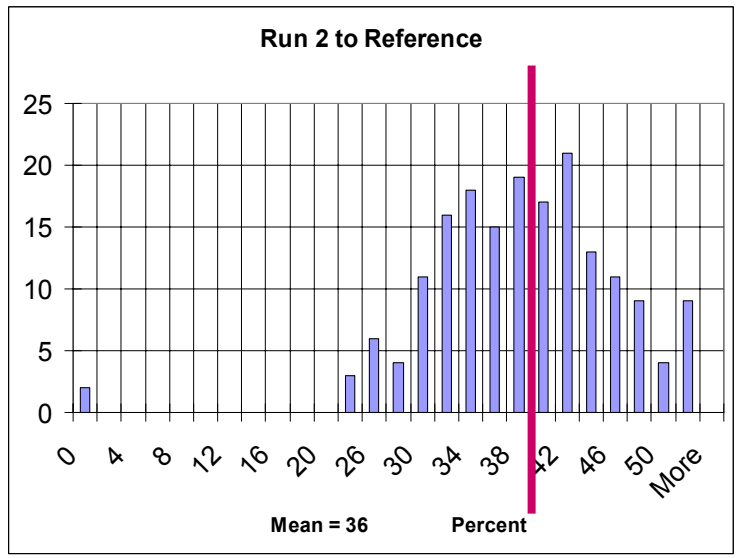
Date of Performance Test	Description of Mechanical/Environmental Test preceding the Performance Test	Performance Test temperature and pressure	Performance Test name or number
07/10/2005	After completion ACD integration		Reference
07/13/2005	After Z-axis vibration along OZ		Post-Z
07/16/2005	After completion all vibration tests		Post-vib
07/21/2005	Pre-thermal tests after completion all mechanical tests	Ambient, normal pressure	Pre-thermal
07/24/2005	After hot survival	Ambient, vacuum	1
07/26/2005	During max cold operational	-25C, vacuum	2
07/27/2005	During max hot operational	+35C, vacuum	3
07/28/2005	During max cold operational	-25C, vacuum	4
07/29/2005	During max hot operational	+35C, vacuum	5
07/29/2005	During max cold operational	-25C, vacuum	6
07/31/2005	During max hot operational	+35C, vacuum	7A
08/02/2005	During max cold operational	-25C, vacuum	8
08/03/2005	At expected operational	0C, vacuum	9
08/04/2005	Ambient	Ambient, vacuum	10
08/05/2005	Ambient	Ambient, normal pressure	11

Test Results

MIP peak position – difference between test 11 (after completion of all tests at GSFC) and reference. We accept mip peak variation by ±10% - looks good



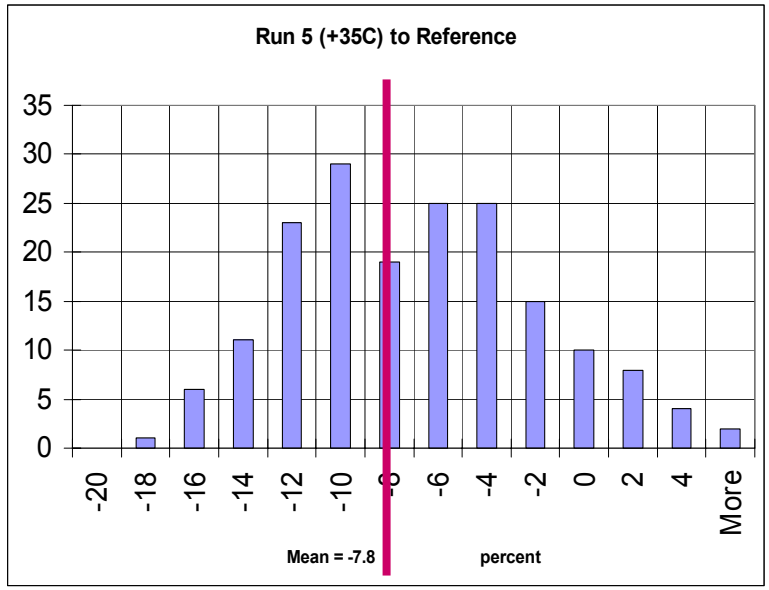
Thermal variation: mip peak position difference between -25C and reference (ambient, 23C). Signals increase by 0.8-0.9%/degree C, exactly as we measured two years ago during ACD design



Test Results (cont.)

Again mip peak position thermal variation – now at increased temperature (+35C), or 12C higher, caused ~10% of mip peak position decrease – same 0.8-0.9%/degree C

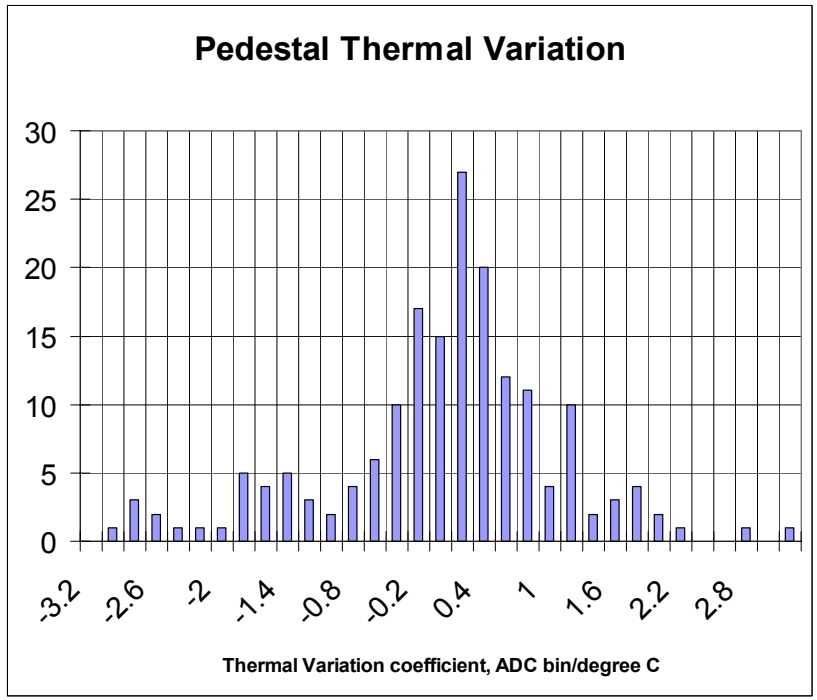
Rough estimate of temperature monitoring in flight: we want to set VETO thresholds (in off-line analysis, where it has to be more precise) with the precision of better than 0.05 *mip*. This corresponds to a maximum 7C temperature change, and to the requirement that the temperature stability has to be monitored with 5C precision to maintain 0.05 *mip* VETO (off-line) threshold stability



Pedestal Thermal variation

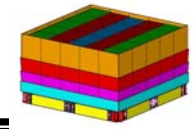
We found that pedestals stay stable (within 2-3 ADC counts) over long time (~ 3 months) if no external changes are made

Pedestals react differently on temperature change: ⟹



Again estimate of temperature stability in flight: similar to *mip* peak position estimate. Assuming we need 0.05 mip peak position knowledge, this corresponds to a minimum of 20 ADC bins. For the worst channels with largest pedestal thermal variation coefficients, this corresponds to ~10C temperature monitoring accuracy. This is a weaker requirement than for *mip* peak position (5C).

Veto threshold thermal behavior



We conducted extensive analysis of VETO threshold behavior with temperature change. Results are placed in large spreadsheet and can be available by request.

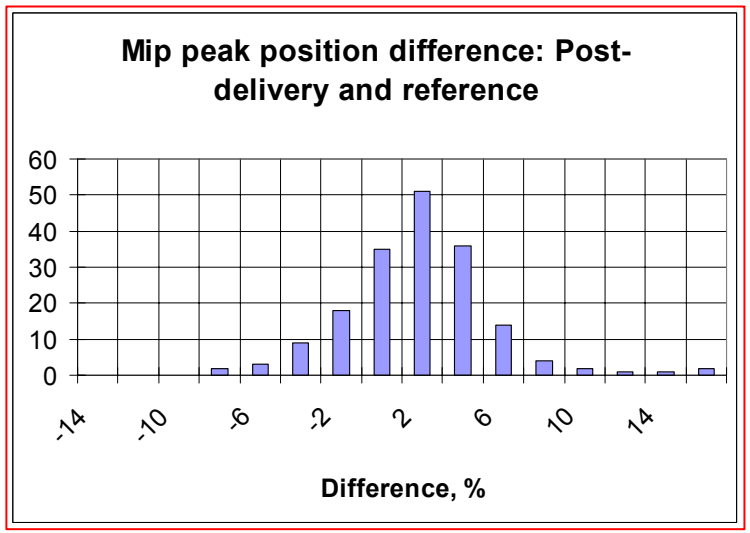
Conclusion for the temperature monitoring – re-calibration (use of different VETO setting matrix) is needed if temperature changes by more than 8-10C

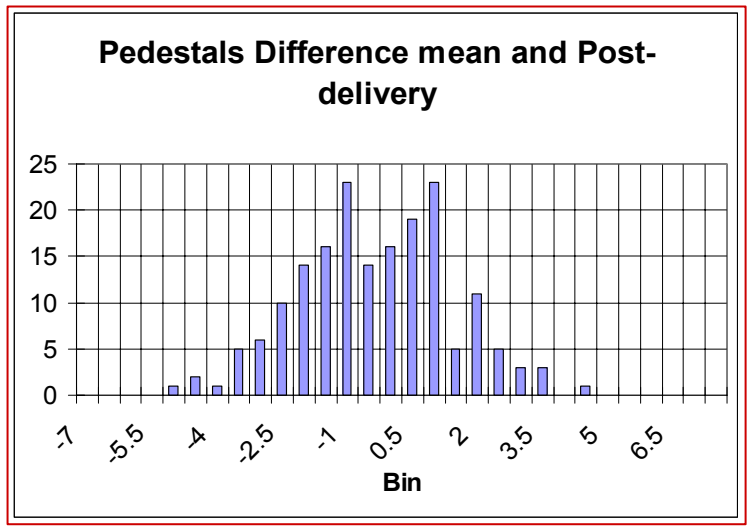
Combining all thermal tests: ACD Calibration parameters have to be created for every 10C temperature range

Moving to SLAC

ACD passed pre-ship review and was shipped to SLAC in the middle of August 2005

ACD post-delivery tests at SLAC demonstrated excellent stability of mip peak positions and pedestals position





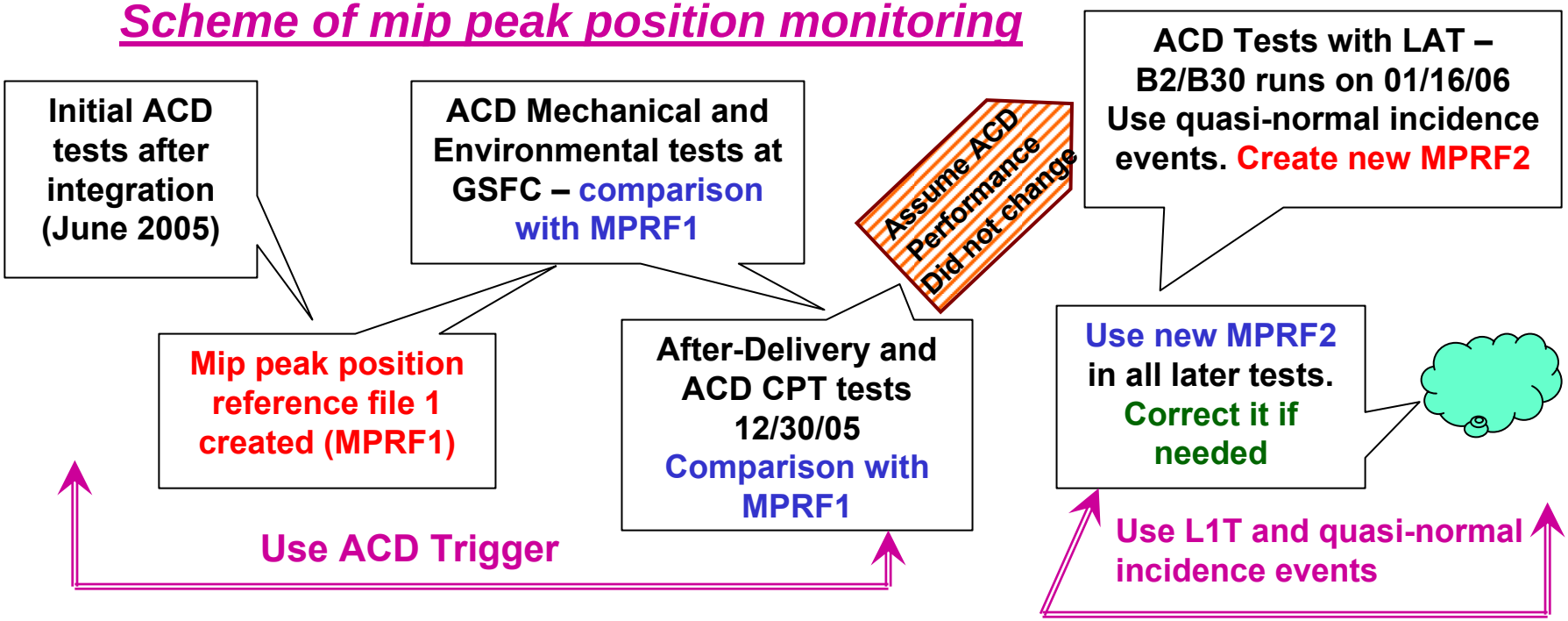
Now we are moving to ACD tests being a part of LAT

MIP Peak position monitoring

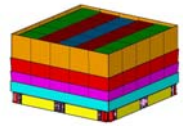
During ACD standalone tests we used TrigOps test to determine mip peak position for every tile. ACD trigger was used for triggering, which allowed about ±30 degrees of incident angle variation. This overestimates mip peak position due to presence of large particle paths in the tile

Use of the tracking information allows to select quasi-normal incidence events and makes mip peak position determination be independent on the test conditions (triggering and incident flux). But it moves mip peak position on PHA histogram to the left and creates disconnection in mip peak position monitoring

Scheme of mip peak position monitoring



MIP Peak position monitoring (cont.)



Now only with using L1T trigger (3-in-a-row) and selection of quasi-normal incidence events:

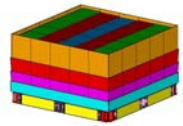
Mip peak position is determined very well for the top tiles because of many of events cross ACD tiles under quasi-normal angles

Calibration of side tiles is not so obvious (especially 3-rd row tiles) because of small fraction of events crossing side tiles under quasi-normal angles

Side tiles: There is a possibility of correcting pulse-heights by the particle path length in a tile. I'd like to avoid using this approach for large angles because of seemingly mip peak position underestimate with this technique for large angles. Eric Charles will discuss path length correction for large angles

Side tiles calibration in flight: Assuming LAT trigger with engine 9 (leaking protons), running with 256 prescale, we will need about 150 hours of total running time to get enough statistics to calibrate side tiles, or 30 minutes without a prescale

Tiles Light Yield



• **Light Yield for all ACD Tiles was measured in the laboratory before ACD integration**

• **Light Yield was measured directly for 3 top tiles (6 PMTs, or channels) and propagated to all other tiles:**

First the average ADC sensitivity A_{fl} was measured using directly measured light yield LY_i for 6 channels:

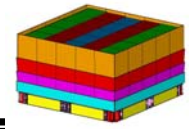
$$A_{fl} = \frac{1}{6} \times \sum_{i=1}^{6} \frac{P_i}{LY_i \times G_{i,fl}}$$

where P_i and G_i are correspondingly *mip* peak position and PMT gain for *i*-channel

Light Yield LY for every channel was calculated according to:

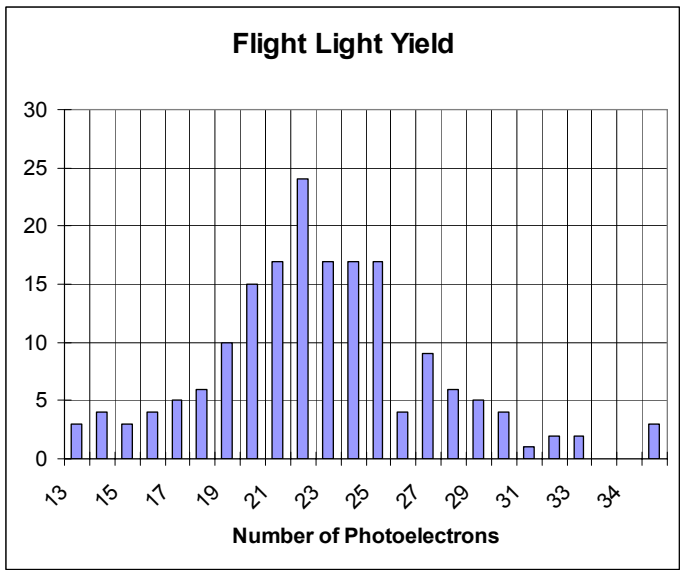
$$LY = \frac{P}{A_{fl} \times G_{fl}}$$

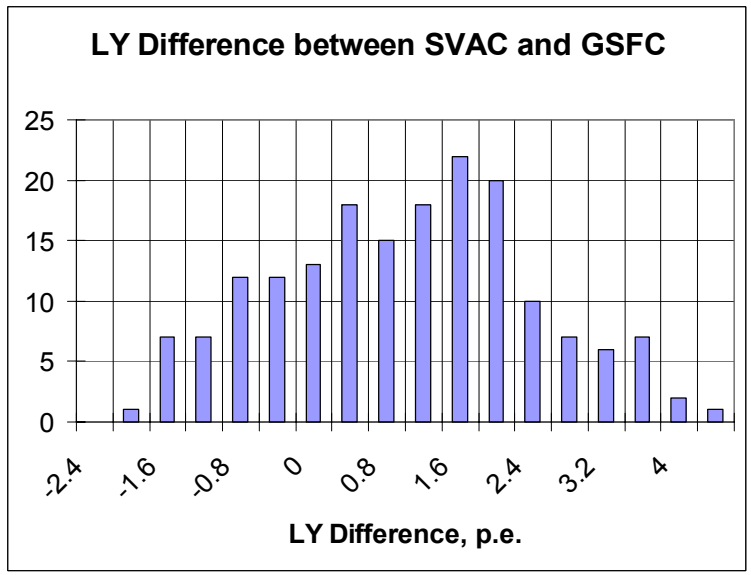
Tiles Light Yield



Now we determined Light Yield for every tile, using SVAC runs at SLAC:

- Using Light Yield determined directly for each of top tiles (50 PMTs, or channels, see Luis Reyes talk for details), we again determined ADC sensitivity ***A***
- Using determined ***A***, we calculated Light Yield ***LY*** for every ACD channel, including that were used for ***A*** determination (top tiles)





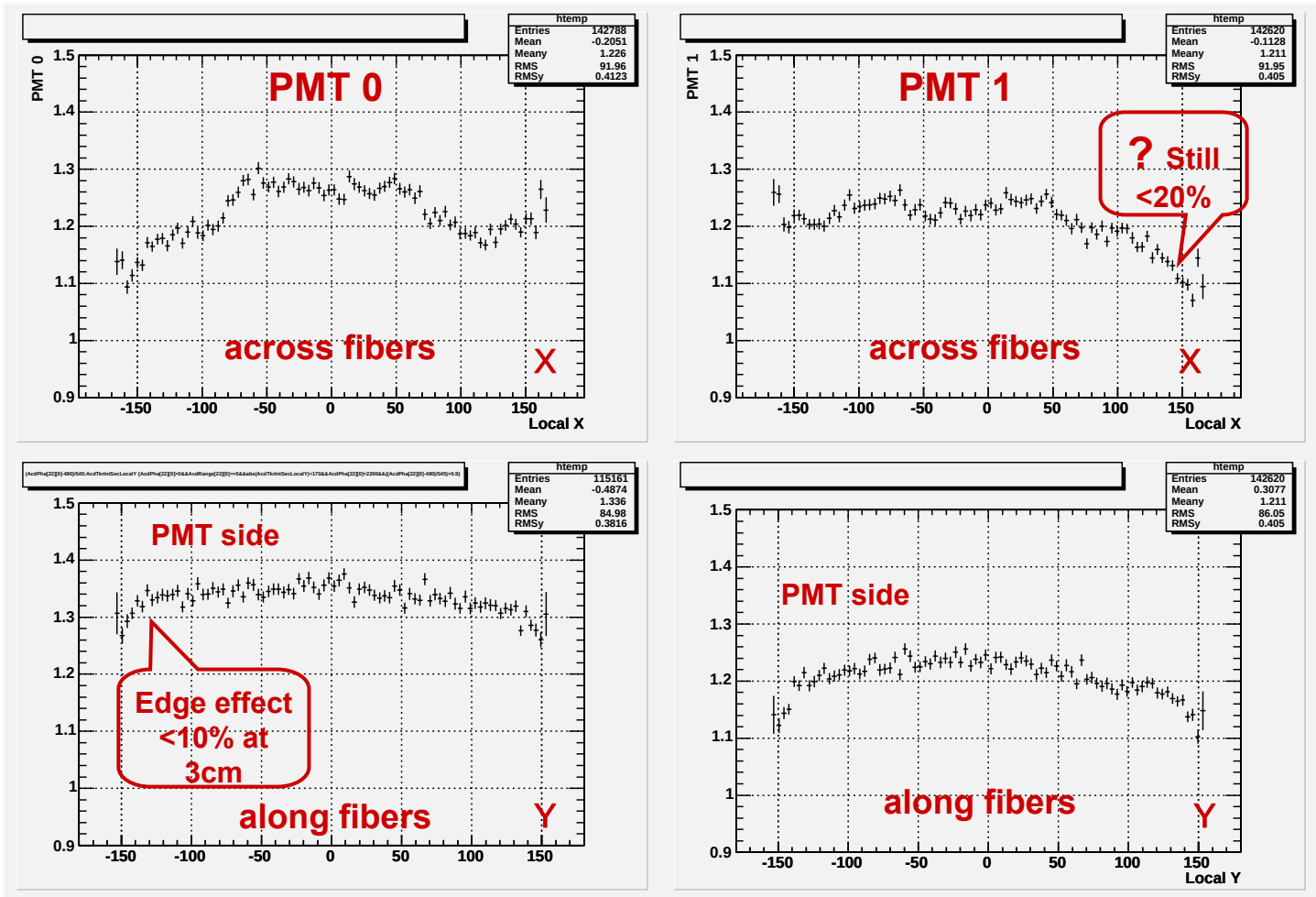
LY **for every ACD channel (PMT)**

Average = 22.2 p.e.

Difference between *LY* measured at Goddard, and measured at SLAC (0.8±1.4 p.e.) Two independent measurements; data analyzed by two different people (Alex and Luis)

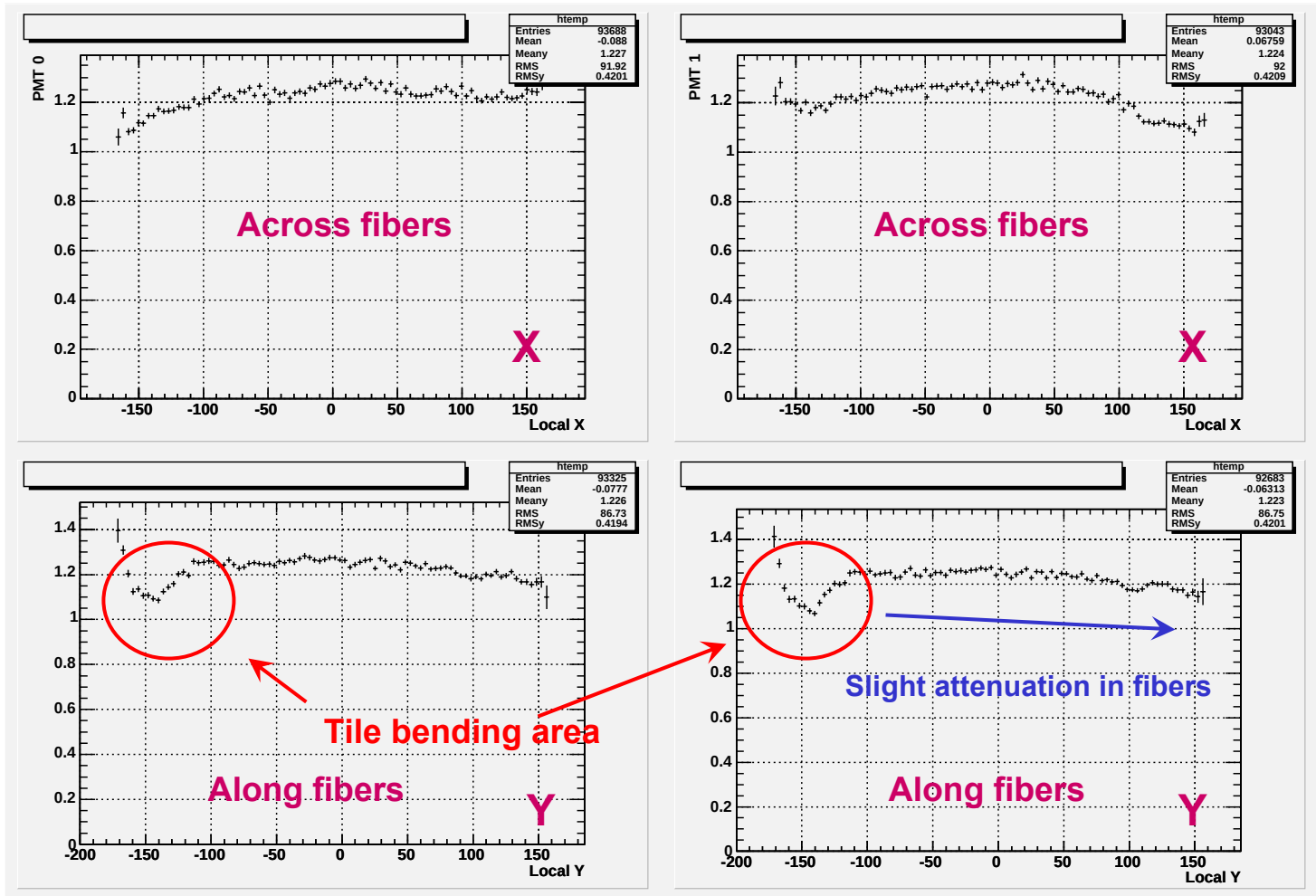
Tiles Light Yield Uniformity

Light Yield across the tile - Example for Tile 22 (very central tile on the top)

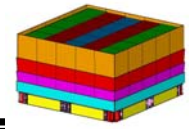


Tiles Light Yield Uniformity (cont.)

Light Yield across the tile - Example for Tile 2 (bent tile on the top)



Tile Light collection – Edge effect



- ✓ Edge effect – light collection reduction toward the tile edge
- ✓ All tiles were checked on the light collection uniformity (tomography)
- ✓ We required the light yield at the tile edge to be not less than 0.7 of that average, with starting decrease not far than 3 cm from the tile edge)
- ✓ We also required that light collection variation across the tile to be within ±10% of its average
- ✓ I am continuing checking tiles light yield uniformity; so far all checked tiles met and exceeded these requirements

Ribbons

- Scintillating Fiber Ribbons cover the gaps between tiles in order to provide detection of the particles which sneak through that gap
- There are 8 ribbons in ACD – 4 run along X-axis, and 4 – along Y-axis
- All ribbons go from one side PMT to the opposite side PMT, which is ~ 3 meters. Thus every ribbon is viewed by PMT at both ends.
- Y-ribbon covers gaps between tiles on the top and on +y and –Y sides; X-ribbons cover gaps on +X and –X sides
- Ribbons provide "per-design" ~ 4 photoelectrons from the event crossing ribbon in the center. Light from any other point of ribbon hit is larger for the PMT which is closer to the hit. Opposite side PMT is redundant in this case. Signals from both ribbon PMTs are Or-ed with the detection threshold of 1 – 1.5 p.e. This corresponds to 30-80 ADC counts depending on PMT

- Due to the strong light attenuation in a ribbon (λ~1.2m), its detection efficiency strongly depends on the hit position.

Ribbons Tests

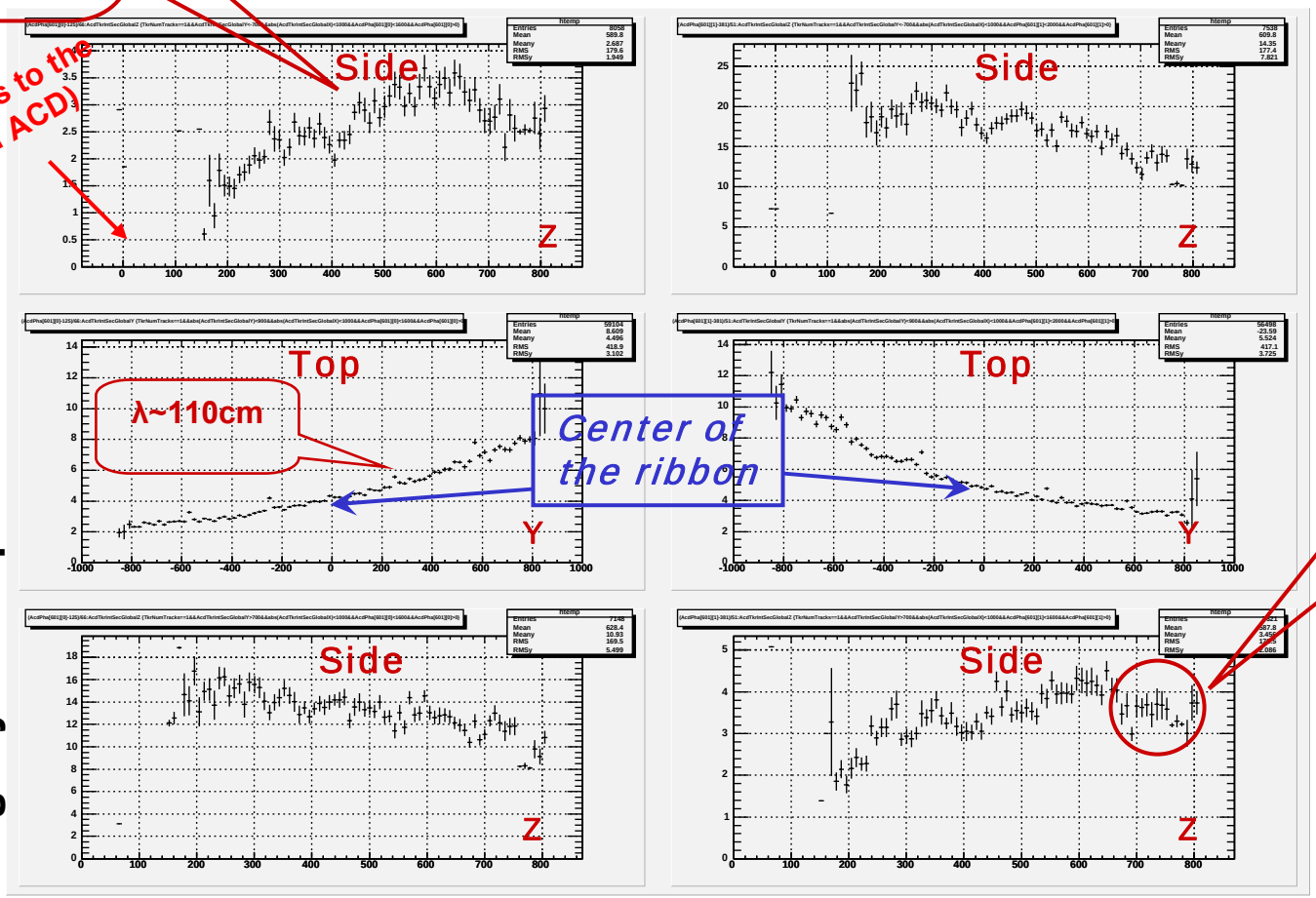
Light Yield along the ribbon 601 - example

Light Yield overestimated along sides due to off-angle paths

Z=0 corresponds to the grid (bottom of ACD)

PMT 0 | PMT 1

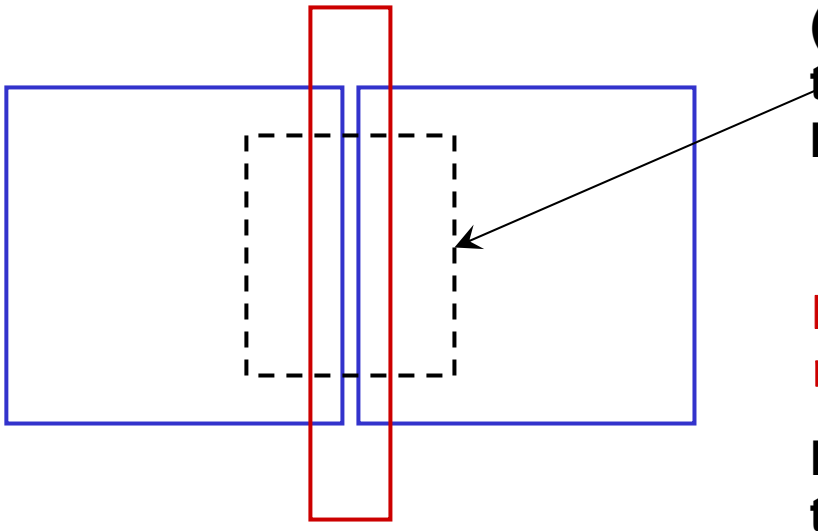
Light yield in photoelectrons



Ribbon part under tile bent

Ribbons Tests (cont.)

Direct determination of ribbons light yield: from B2/B30 ground muon runs



Straight muon selection criteria (see Luis Reyes talk) were applied to the area of 10cm across ribbon by 20cm along ribbon

Example for the center of ribbon 602:

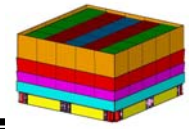
Fraction of events detected only by tiles with threshold 0.3 mip – 0.99

Fraction of events detected by:

Ribbon threshold	One ribbon PMT + tiles	Both ribbon PMT + tiles
1 p.e. (40 counts)	0.9993	0.99966
1.5 p.e.	0.9987	0.99946
2 p.e.	0.9983	0.9993

In order to determine ribbon light yield this geometry was simulated assuming known tiles light yield. Obtained light yield value for this example was 4.8 p.e.

Ribbon Tests (cont.)



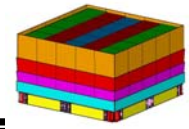
Efficiency was determined for every ribbon in 3 points. Light yield was determined by matching simulations and experimental results, and combined with that determined by the same way as for tiles

Black – as determined in GSFC

Red – current test

Ribbon	PMT	End		Center	End	
500	0	11.1	7.5	4.8	2.0	2.6
	1	2.7	3.2	5.3	12.0	9.0
501	0	10.7	7.9	4.8	1.7	2.8
	1	2.2	2.6	4.4	11.4	7.8
502	0	1.3	1.6	3.0	8.5	5.7
	1	11.9	7.1	4.0	1.1	2.0
503	0	2.3	2.7	4.5	10.0	8.4
	1	11.4	7.7	4.4	1.8	2.4
600	0	10.1		2.8	5.8	3.0
	1	1.6	2.6	4.1	3.9	6.8
601	0	1.6	1.7	4.1	3.1	6.4
	1	8.5	6.6	2.4	4.4	1.9
602	0	8.9	7.3	2.7	4.4	2.4
	1	1.7	1.9	3.8	4.8	7.6
603	0	1.5	2.5	3.8	4.7	9.2
	1	12.9	8.8	3.3	4.1	2.3

Ribbons - conclusions



- Ribbons performance meet requirements to provide required ACD efficiency – will be shown later
- Obtained ribbons light yield values can be used in simulation model
- Suggested detection threshold for the ribbons is 1 p.e., which corresponds to from 30 to 80 ADC counts

Situation: Such a low threshold can create false Veto

Selecting given area (see slide 11) – no one ribbon yielded signal above 1 p.e. threshold. It was checked for many areas – same result. Detection threshold of 1 p.e. is safe

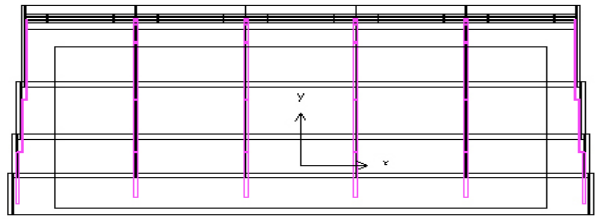
Whole ACD Performance Simulation

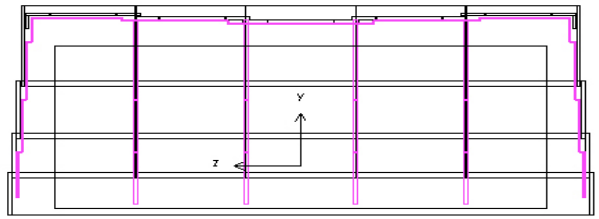
Whole ACD performance was simulated by Geant 3

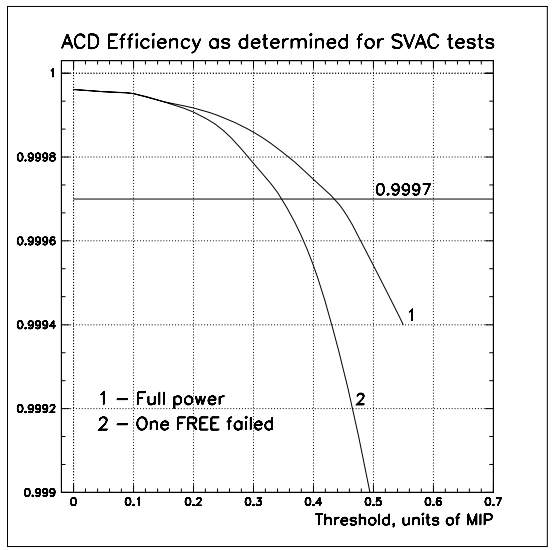
Isotropic flux of incident particles was used

All gaps correspond to -20C (lowest expected operational temperature, worst case)

Light Yield for tiles and ribbons are taken as measured in SVAC tests



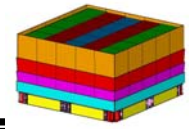




ACD has an overall efficiency of ≈0.99985 at VETO threshold of 0.3 mip and ribbons threshold of 1 p.e.

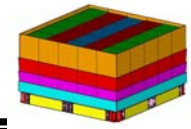
Failure of one FREE board – up to 18 tiles run with single PMT – still OK

Conclusion



- Now we have in our hands all needed ACD parameters
- We have a clear scheme of ACD parameters monitoring
- And, of course, there are always some new things are found. We need to understand their nature, but the main thing is to determine their impact on ACD required operation, and, if these new found effects do affect ACD operation, find out how to tolerate them

A Reminder about ACD Calibrations



Essentially none of the tests done on the ACD on the LAT have been done in a flight-like configuration:

1. The flight configuration planned only one of the two sets of VETO drivers enabled.
2. Testing has largely been done with both sets enabled.
3. Using both sets reduces the voltage on the ACD electronics by about 0.1 V, putting it close to the lower limit of the ACD operating range.
4. The ACD pedestals are voltage-dependent, so this lower voltage changes the operating points. Such changes differ in both magnitude and sign from channel to channel.
5. Neither the pre-installation calibrations (which were done with a different GASU) nor any calibrations that have been run in this non-standard configuration necessarily represent the ACD as it will be operated in flight.
6. A flight software change is needed in order to turn off one set of drivers (the power-on default is both sets on).
7. Once this change has been made, we need to re-run all the calibration scripts for the ACD and adjust operating parameters accordingly.