GLAST Large Area Telescope

LAT MRB for ACD FREE Board

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Statement of Problem

- A mode has been found where the GARC ASIC on the ACD FREE board has the potential to power up in a stuck-at-reset mode
- This problem was documented in a Goddard Problem Report, ACD-0-001, on 15 January, 2004.
- This mode has been shown to happen at an unacceptable rate in the flight configuration, and it has been determined that a fix is required

Root Cause of Problem

- The root cause of the problem is a design flaw in the GARC ASIC. There are flip-flops in the RESET deglitch processing circuitry that do not have explicit reset inputs. These flip-flops can power up in an indeterminate state.

- The RESET flip-flops on the unpowered DAQ side never receive clocks and therefore are never cleared, causing the GARC to remain in RESET mode.

Proposed Solutions

	Proposed Solutions	ACD Cost	ACD Schedule
1	Modify Existing FREE Cards - Add passive components to the existing FREE card to work around the turn-on problem. (No schedule impact due to delays in delivery of GARCs) - see next slide for variations to this option	<10k Time to test fix	None
2	Make New FREE Cards - Add active components to FREE that may fix the reset problem. The re-design of the FREE card is being done. We consider this approach to be a back-up.	114k + Marching army	3 months/ 1.5 months RFI variance
3	Make New GARC	110k + Marching army	5 months/ 3 months RFI variance

Proposed Solution 1 Variations

Three Variations to modify existing FREE cards:

1. Wire-OR the primary and redundant driver circuits. This approach was documented in

   http://lhea-glast.gsfc.nasa.gov/acd/electronics/free/FREE_Board_Reset_Fix.pdf

   A concern is that some level of redundancy is removed by the modification.
2. Cross-strap the clock and reset inputs to allow a portion of the transmitted signal to be seen by both sets of receivers (suggested by Oren Milgrome). This approach, which requires addition of 2 resistors to the existing FREE cards, is documented in
   http://lhea-glast.gsfc.nasa.gov/acd/electronics/free/GARC_Reset_MRB_Report_030504.pdf
3. A variation of 2. using four resistors and a capacitor, to reduce possible noise on the unpowered line. Because it involves adding five components instead of two, we consider this a backup if noise is observed in testing 2.

Selected Solution – Adding Components to FREE Card

- It is necessary to provide at least several clocks to both the "A" side and the "B" side GARC receivers after the power-on reset is deasserted to ensure proper startup.

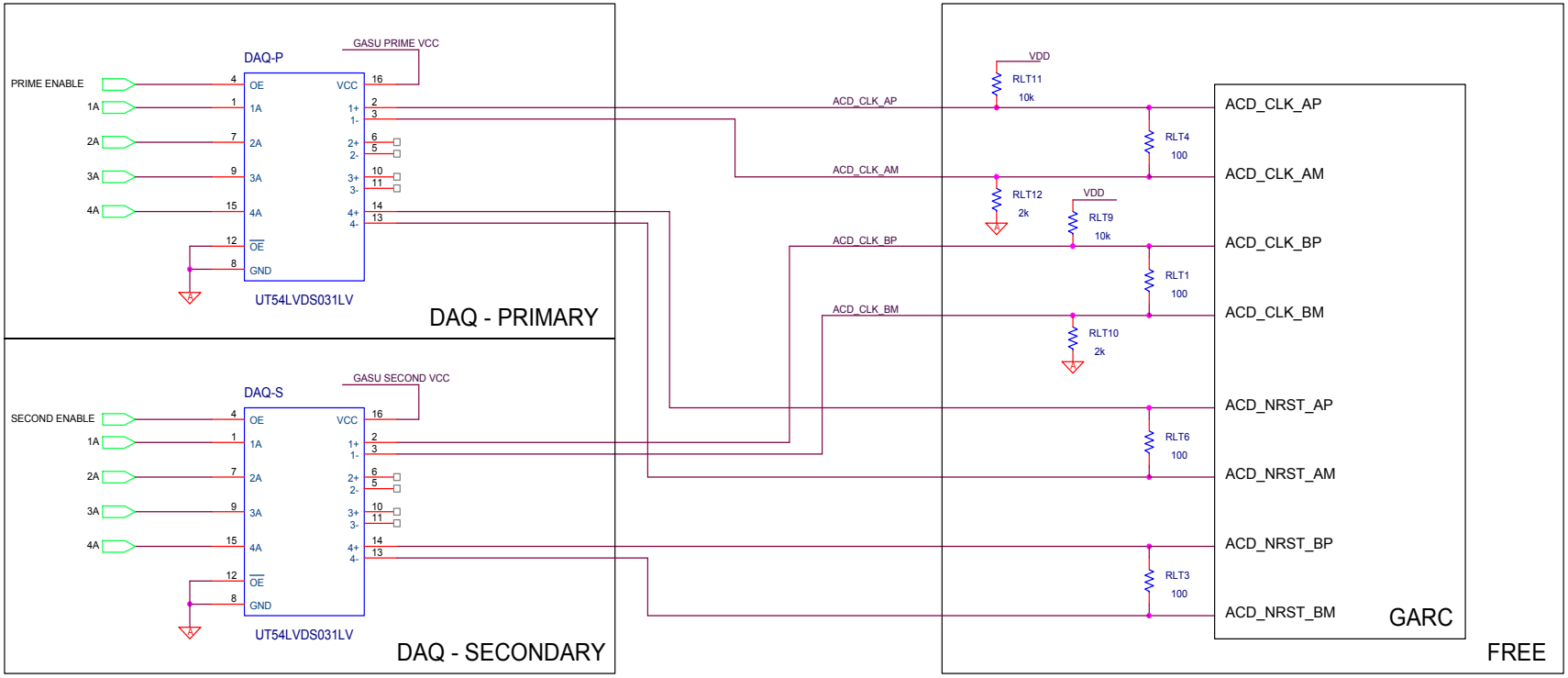
- A solution is presented to provide resistive cross-strapping of the GARC receiver circuits to provide the required clocks – Variation 2 from previous chart.

- A change in the GASU will also be required.

Present Circuit

The proposed modification involves cross-strapping the clock and reset inputs to allow a portion of the transmitted signal to be seen by both sets of receivers. The circuit as it presently exists on the FREE card is shown below

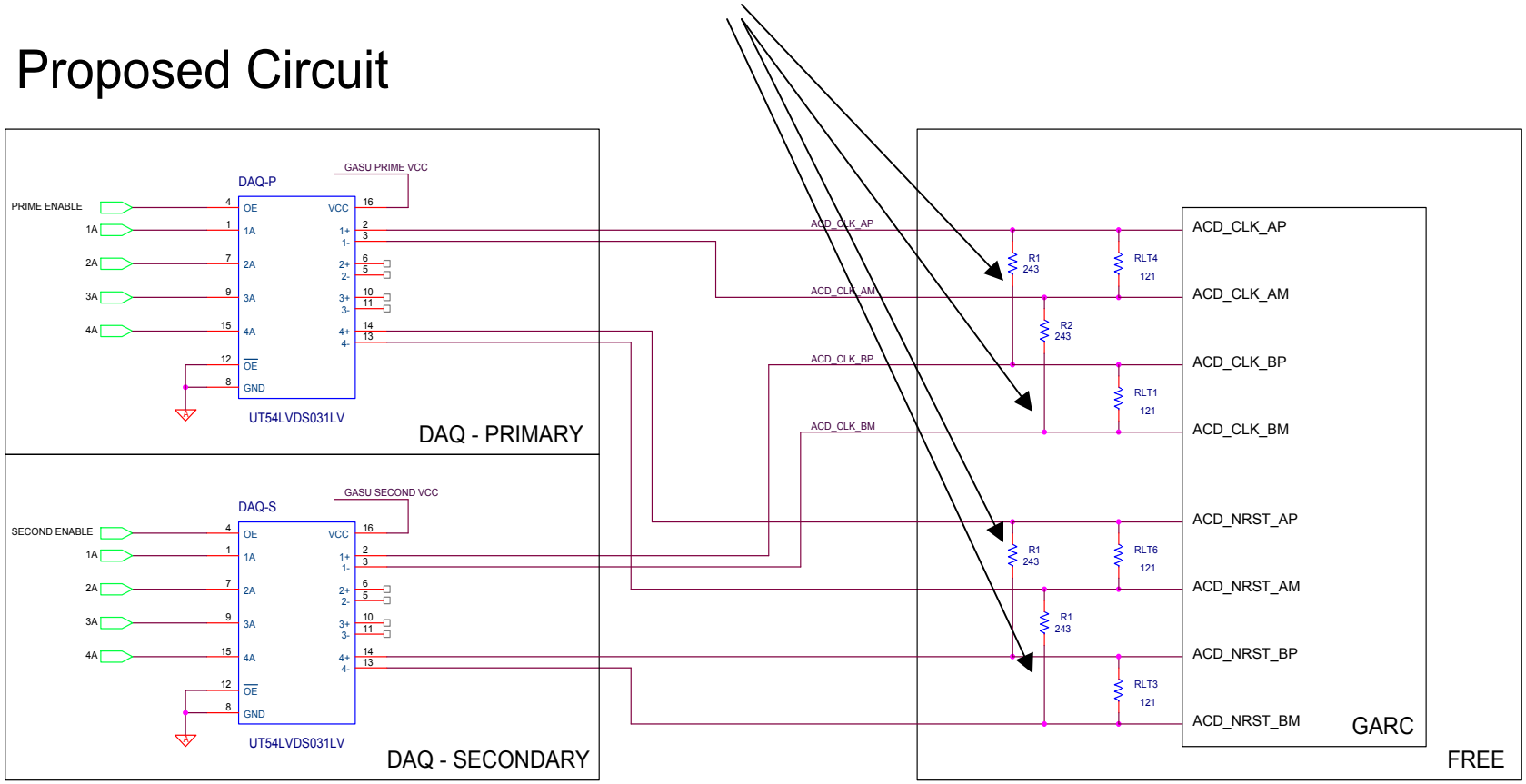
Present Circuit



Schematic of Proposed Fix

The 243 ohm resistors show the cross-strapping between the receiver pairs

Proposed Circuit



Impedance Calculation

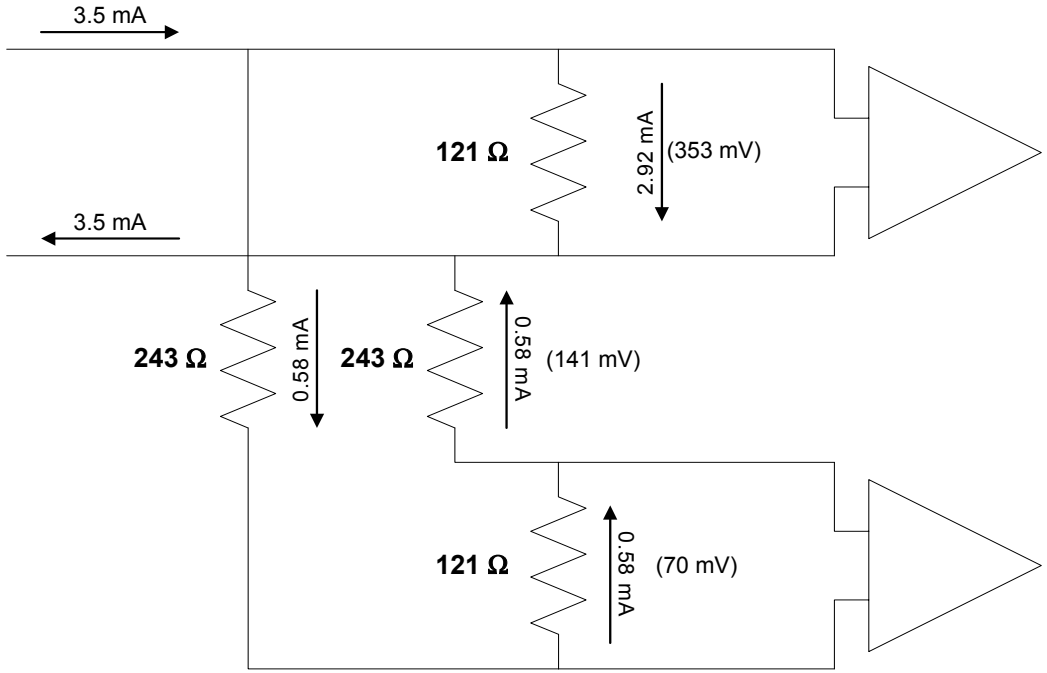
Total termination impedance using the 121 Ω resistors at the receiver inputs and the 243 Ω cross-strapping resistors is:

$$Z = \frac{(121)(243+121+243)}{121+243+121+243} = 100.9\Omega$$

which is close to the desired 100 Ω termination.

Current and Impedance Calculations

The calculated signal amplitudes based on nominal LVDS currents are shown below:



The primary (powered) receiver maintains the ~ 350 mV signal across the 121 Ω resistor with 2.92 mA of (nominal) current. 580 μA current is shunted through the 243 ohm resistors and the redundant (unpowered) receiver. This provides ~ 70 mV of difference across the unpowered receiver, which is enough to toggle the GARC receiver in the absence of cabling reflections.

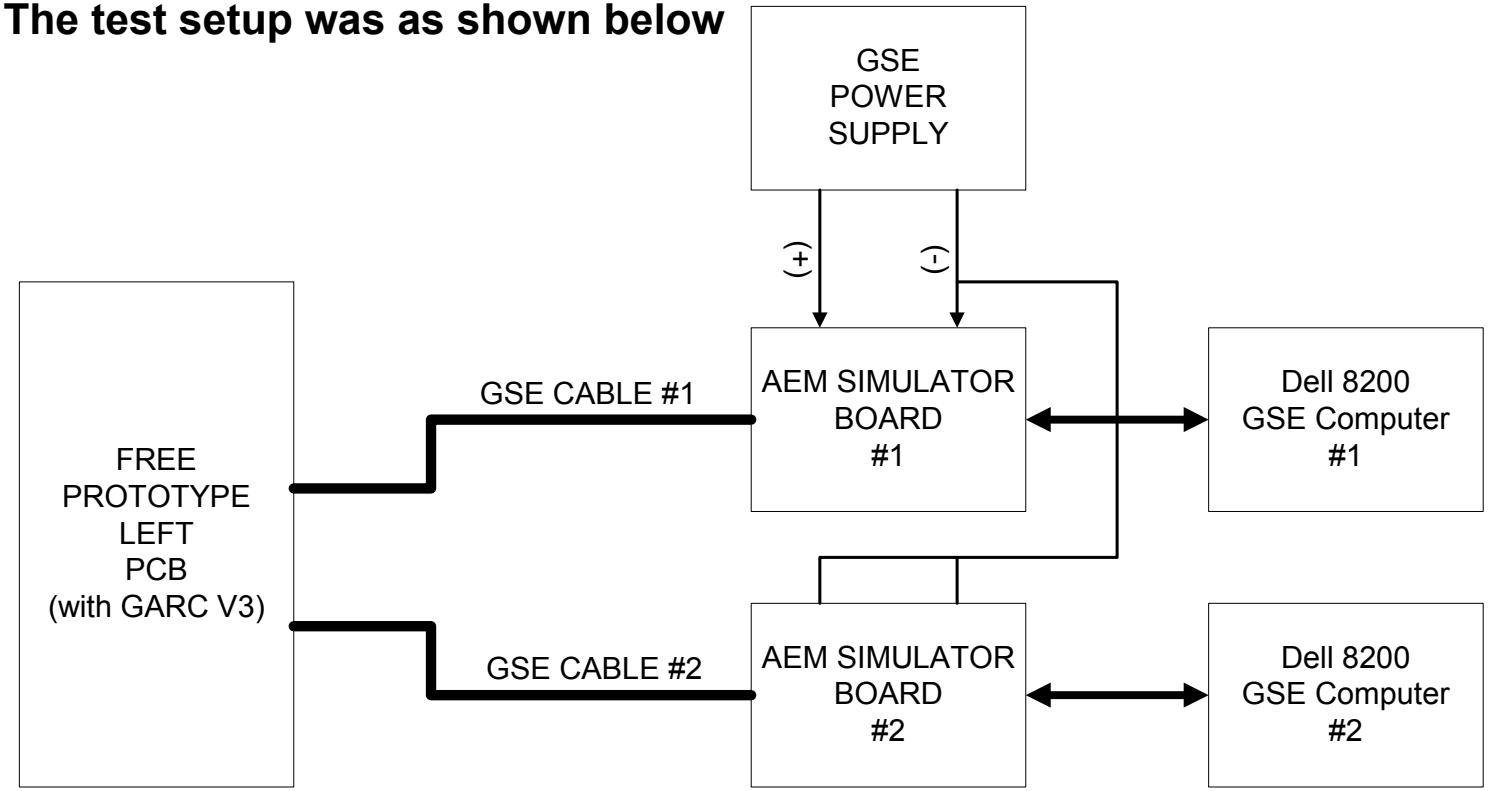
Reflections in the Cabling

- Cabling reflections from the unterminated, unpowered driver side are quite significant with flight length cables.
- **At the nominal 20 MHz clock rate, this fix does not function reliably**.
- LAT Electronics has agreed to configure the GASU to drop the clock rate to approximately 1.25 MHz for 1 second at FREE board turn on to mitigate this problem.
- At the 1.25 MHz rate, the reflections do not hinder operation and the FREE card redundant (unpowered) receiver will receive clocks reliably (which is the goal of this modification).
- After 1 second, LAT will command the GASU to return the FREE card clock to the nominal 20 MHz rate for operations.

The proposed change is to be made on both the clock and the reset signal paths. If both the primary and redundant clock receivers can be active, it is necessary to ensure the reset level is held inactive.

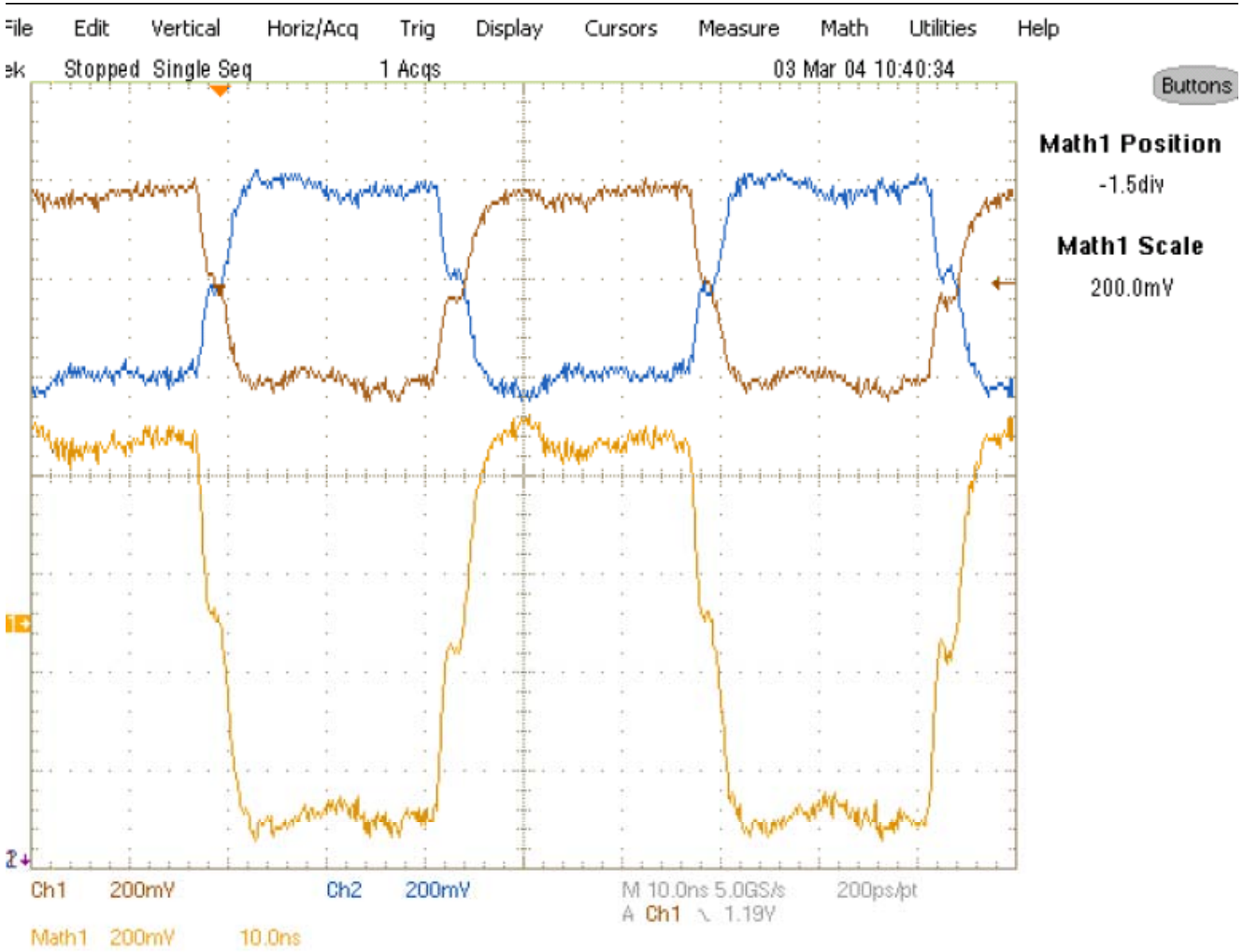
Test Setup at Goddard

This modification has been tested on the bench with a setup that is similar to the flight configuration (we plan to retest with the GASU when it becomes available). The test setup was as shown below



In this setup, AEM simulator board #2 was kept powered off with the power leads shorted together and tied to ground. This is to simulate the redundant (unpowered) DAQ card in the GASU.

Test Results - Signals at the Powered Receiver



FREE PL Board Test
3-3-04

Freq = 20 MHz

Probes at RLT4
powered receiver

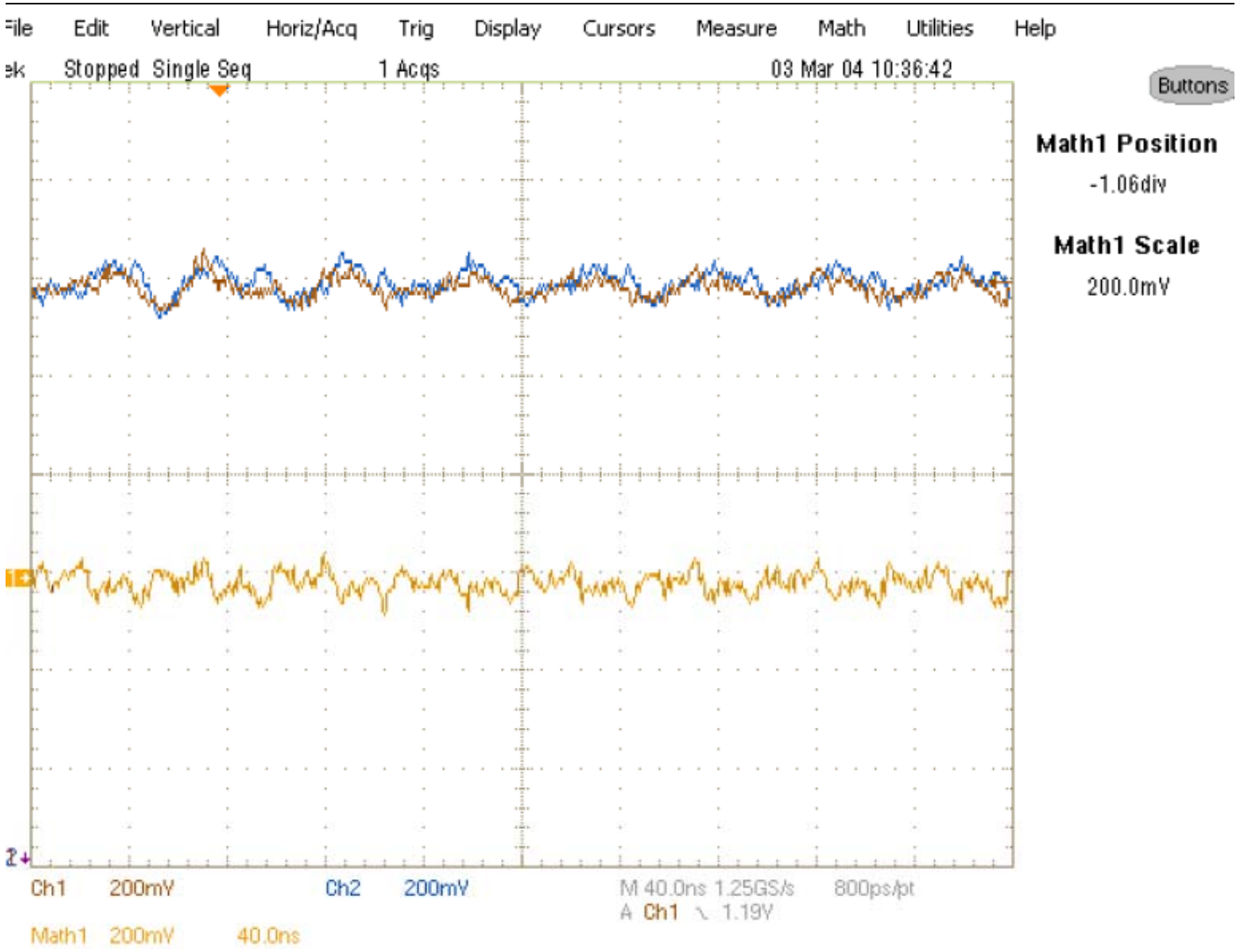
Long cable on
powered driver, short
on unpowered driver

Timebase 10 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 100 mV/div
is the differential
seen by driver

Powered receiver, 20 MHz, Differential signal is ~ 700 mV

Test Results - Signals at the Unpowered Receiver



FREE PL Board Test
3-3-04

Freq = 20 MHz

Probes at RLT1
unpowered receiver

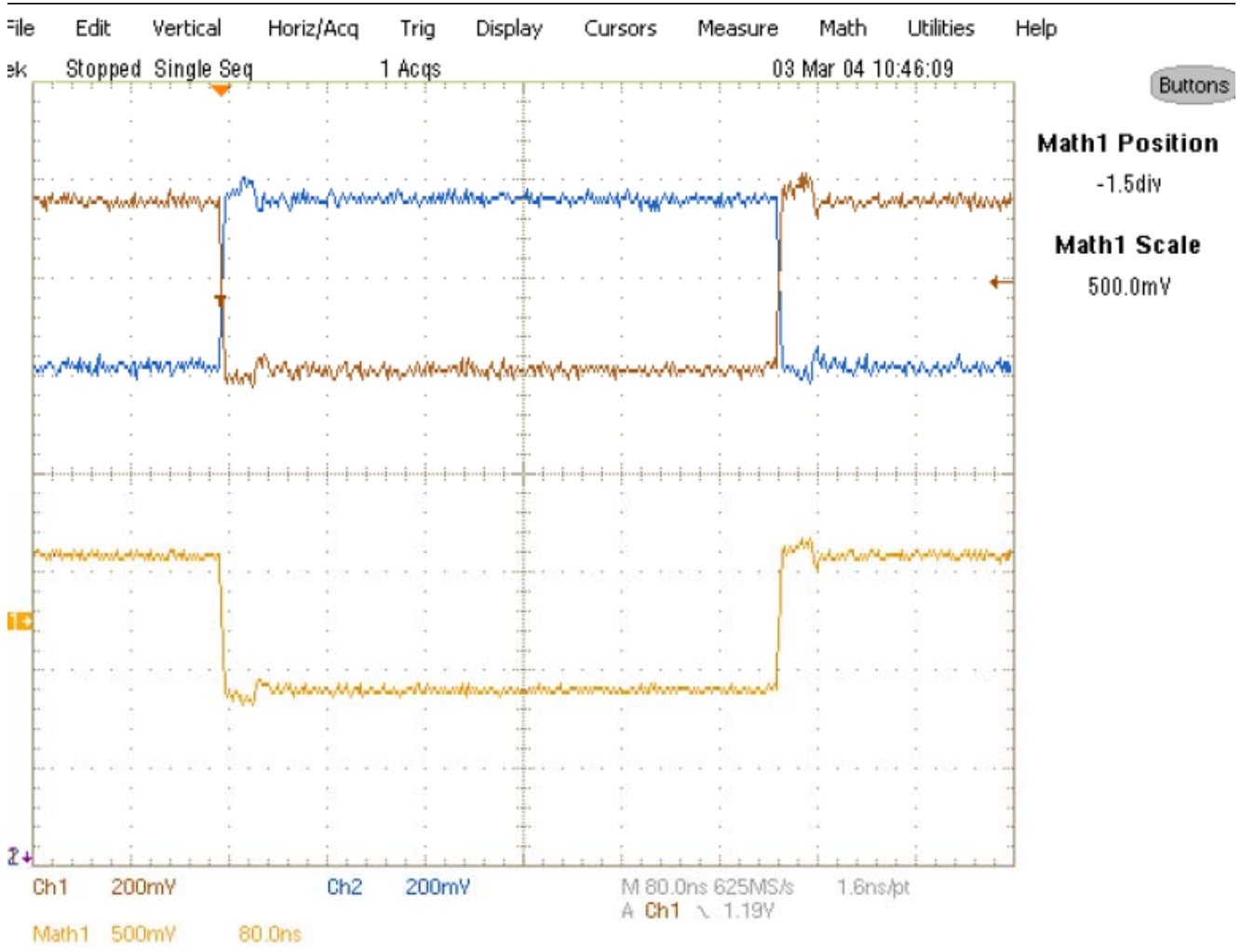
Short cable on
powered driver, long
on unpowered driver

Timebase 40 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 200 mV/div
is the differential
seen by receiver

Unpowered receiver, 20 MHz.
Implementation has no margin at 20 MHz as tested.

Test Results - Powered Receiver at 1 MHz clock



FREE PL Board Test
3-3-04

Freq = 1 MHz

Probes at RLT4
powered receiver

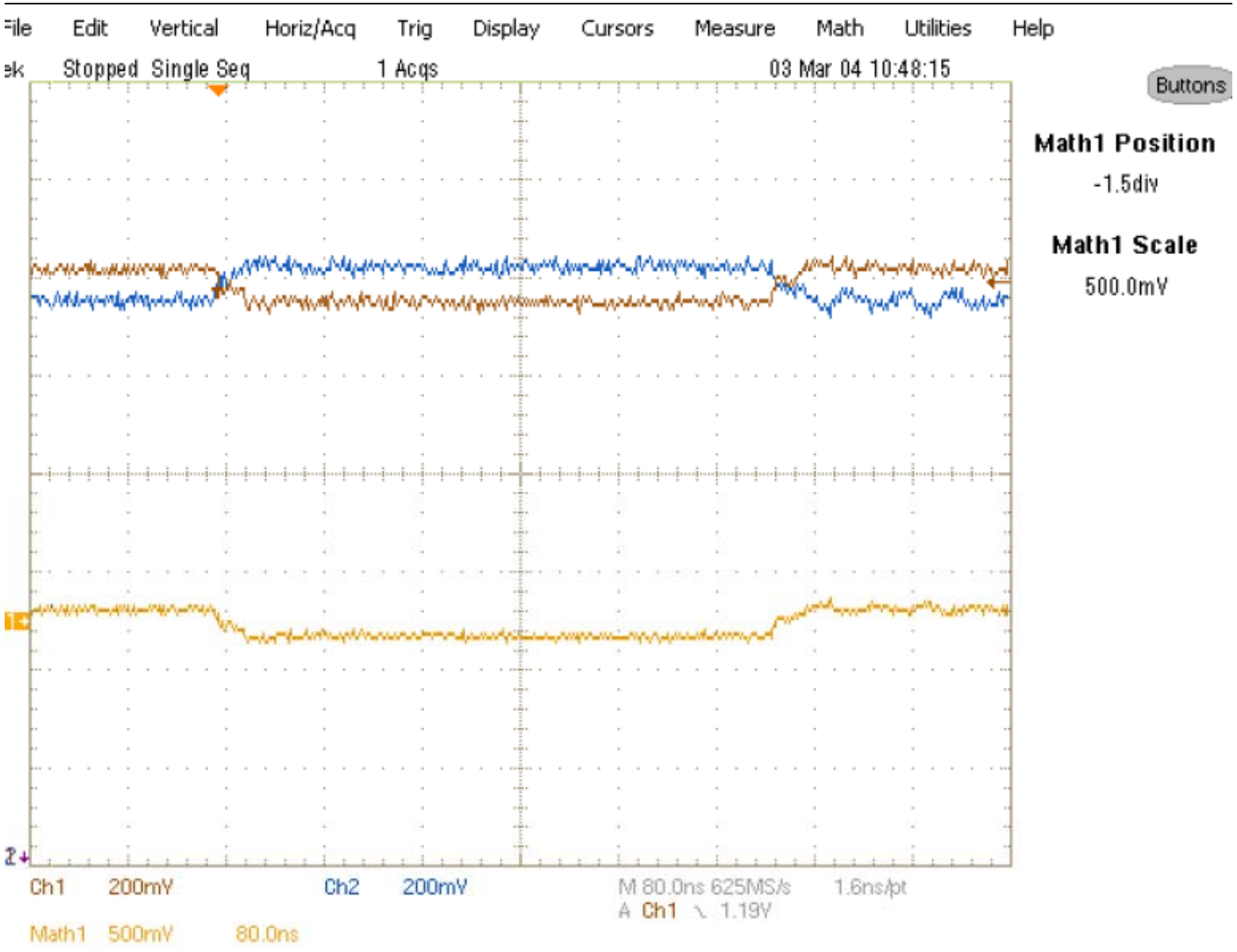
Long cable on
powered driver, short
on unpowered driver

Timebase 80 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by receiver

Powered side, 1 MHz, Differential signal is ~ 700 mV

Test Results - Unpowered Receiver at 1MHz Clock



FREE PL Board Test
3-3-04

Freq = 1 MHz

Probes at RLT1
unpowered receiver

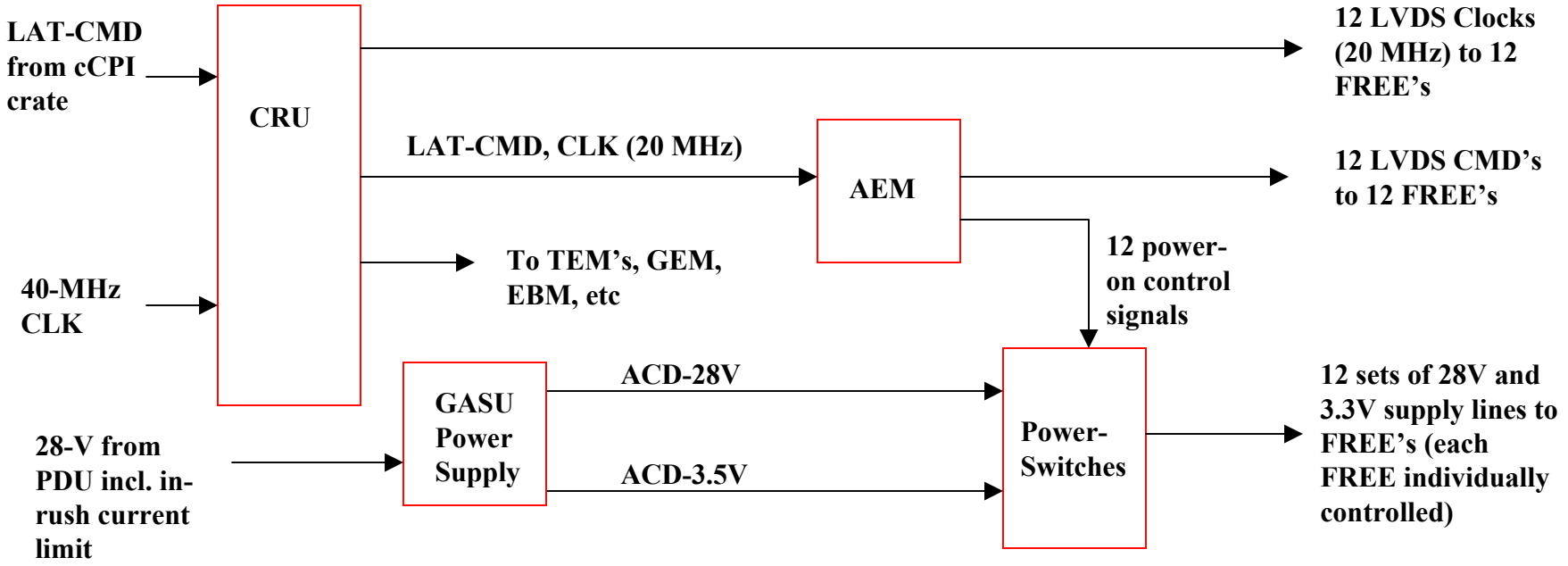
Long cable on
powered driver, short
on unpowered driver

Timebase 80 ns/div
Ch 1 @ 200mV/div
Ch 2 @ 200 mV/div

Math @ 500 mV/div
is the differential
seen by driver

Unpowered receiver, 1 MHz, Differential signal is ~ 150 mV

Baseline Flight Design of DAQ-GASU

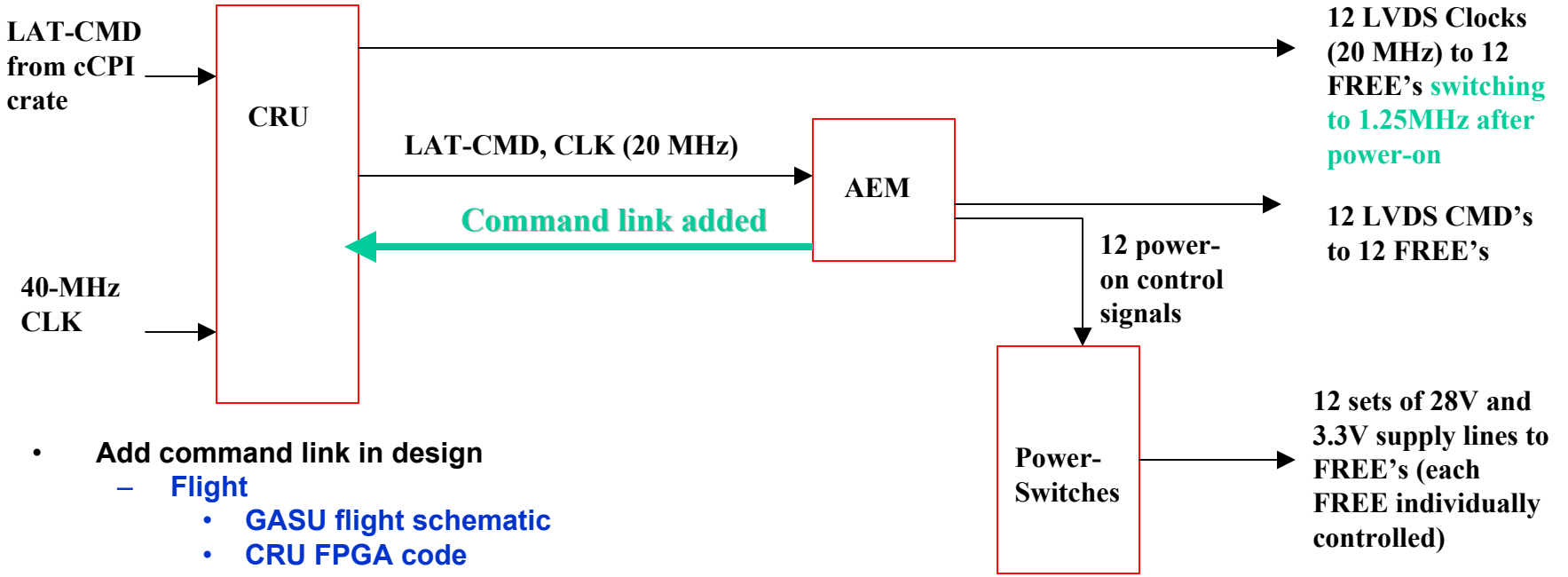


- GASU contains
  - Event-Builder Module (EBM)
  - Global Trigger Module (GEM)
  - Command-Response Unit (CRU)
  - ACD Electronics Module (AEM)
  - Figure shows simplified GASU
- AEM contains all ACD registers/control/read-out decoded from LAT-AEM command line
  - Includes ACD power-on registers -> controls power to 12 FREE cards individually
- CRU
  - Origin of 20 MHZ clock to FREE's (due to clock-skew requirements)

New Requirements

- Switch FREE clock frequency from nominal 20-MHz to 1.25 MHz for about 1-sec following power-on to FREE
- Problem
  - Clock comes from CRU
  - Only AEM knows when FREE's are powered
- Preferred Solution
  - Add path from AEM to CRU to communicate power-on transition
    - Can't use already available 12-FREE power-on signals on board (digital contamination of signals to base of power-on pnp-transistors resulting in cross-talk into AEM 3.3V voltage), plus need 12 additional pins on CRU
  - Implement as serial command connection from AEM to CRU

New Design of DAQ-GASU



- Add command link in design
  - Flight
    - GASU flight schematic
    - CRU FPGA code
    - AEM FPGA code
  - G3 test-stand
    - Add wires on G3-GASU board
    - Modify CRU and AEM FPGA code
    - Modify software for AEM register control
- Need to see how to test since 1.25MHz clock is only temporary and effect on FREE can not be "read-back"
- Question of
  - "hard-wire" 1-sec 1.25Mhz duration only at power-up
  - Add register in AEM to select frequency independent of power-up

Impact to ACD Document

- FREE Card Schematics
- FREE Card Assembly Drawing
- FREE Card Parts List
- LAT-ACD ICD

The changes to each of these documents is considered to be minimal.

Conclusion/Recommendations

- The ACD and LAT Electronics teams believe that this FREE problem can be mitigated reliably by adding the cross-strapping resistors on the FREE card and the change (20 MHz clock to 1.25 MHz for ~ 1 second) in the GASU
- The ACD team has analyzed the schematic of the GARC receiver and concluded that receiving a clock which might clock only some of the flip-flops in the non-active receiver won't cause a false look-at-me command to occur.
- Assembly of the flight FREE cards can continue with an Engineering Order written to incorporate this modification
- Additional cost and schedule impact to ACD is minimal