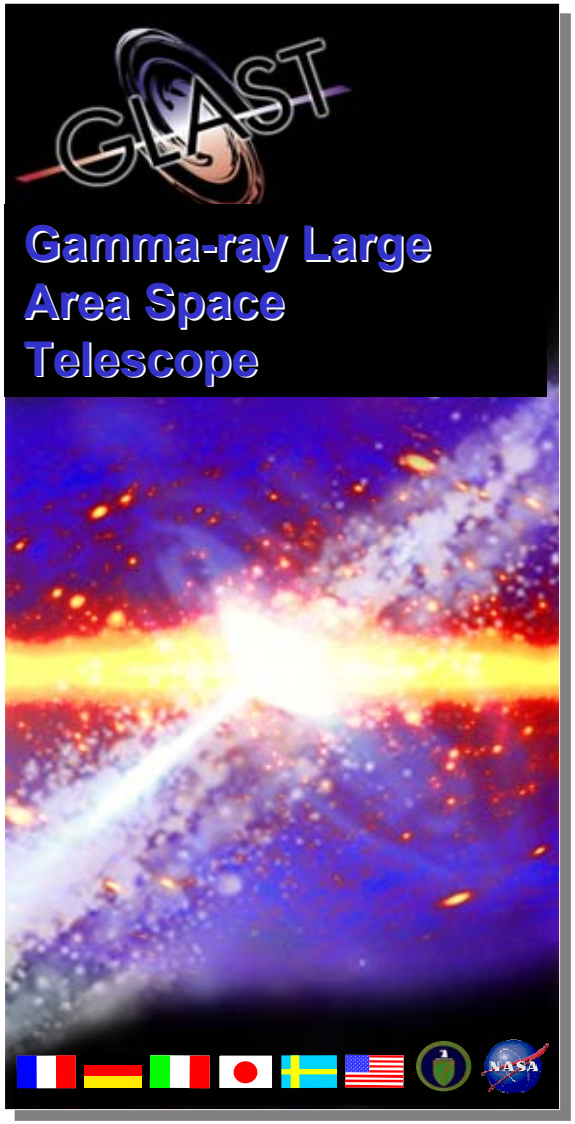

GLAST Large Area Telescope:

Electronics, Data Acquisition & Flight Software W.B.S 4.1.7

July 03 Status for July 27, 03 Meeting

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July Accomplishments

- GASU tests continued
- PDU back from fab, loaded, in test
- Designed alternative tower supply solution, being simulated
- TEM with ASICs (flight model) back from board fabrication, loaded
- Submitted requisitions for several flight-parts
- Radiation tested (SEU, SEL) of DAQ ASIC's (GCCC, GTCC, GLTC) at Legnaro
- Interviewed candidates for Joby replacement (DAQ packaging engineer), issued offer letter, was accepted, start date mid August.

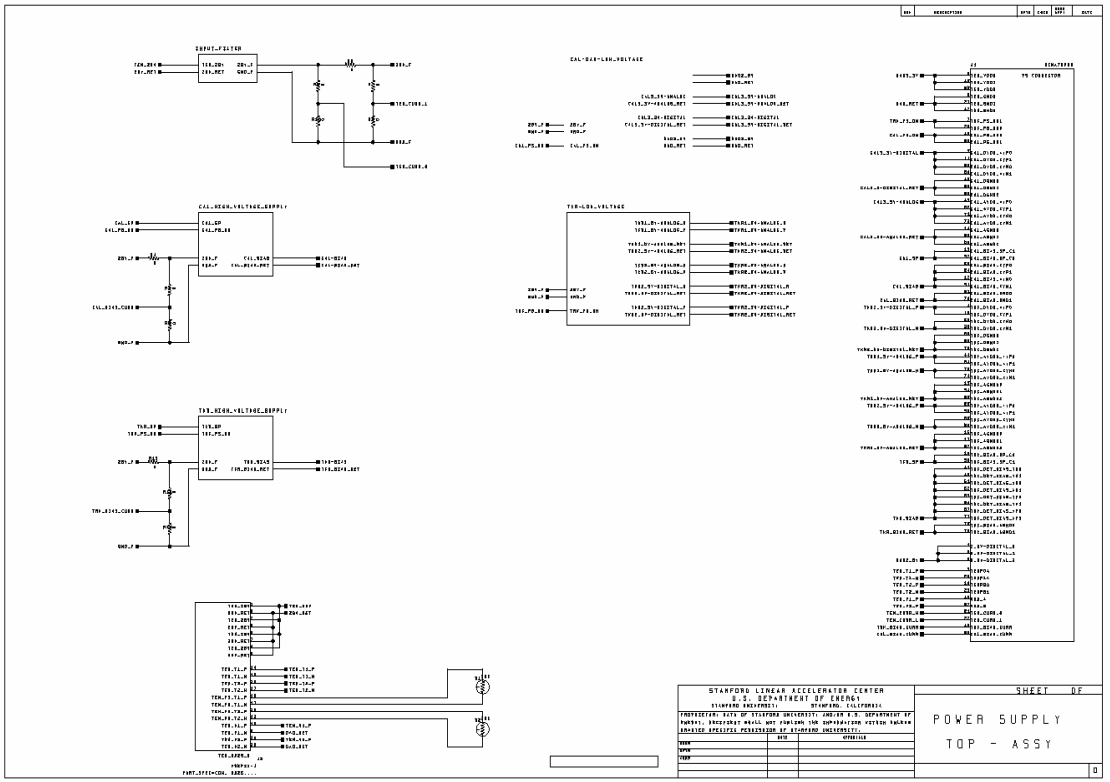
- Worked on filter output data compression (looks like factor of 2)
- First boot code committed to SUROM on RAD750 and tested
- Review of command & telemetry document
- Upgrade to VxWorks 5.5 almost complete
- Worked on update to schedule to get ready for PCMS release
- Provided responses to RFA's of IV&V
- Received and successfully made work SAI spacecraft interface simulator at NRL
- LCB command-response and event path being debugged

Issues and Concern

- Power supply schedule
  - Redesign in progress
  - Radiation tested MAX724/726, passed
- Still concern that 1st prototype of TEM ASICs may not be final flight
  - In test, still ok, but need CAL/TKR front-end with flight-like ASICs to verify performance
- Need to order parts asap, delivery risk
  - Ordering parts almost daily
- Need software help
  - Have descriptions for two additions
  - Goal is to have names of engineers and name of service company to which PO needs to be placed in the next two weeks
  - Need GSFC to be able to place PO asap thereafter
- DAQ thermal/mechanical packaging engineer has left
  - Interviewed candidates, found replacement, will start mid August
- Target DMA disconnect with RAD750 may be too frequent
  - Received additional engineering unit from BAE at SLAC ahead of schedule
  - Have LCB board at stage where it can be tested by mid August
  - Have Ethernet board
  - Will run tests in the later part of August/early September

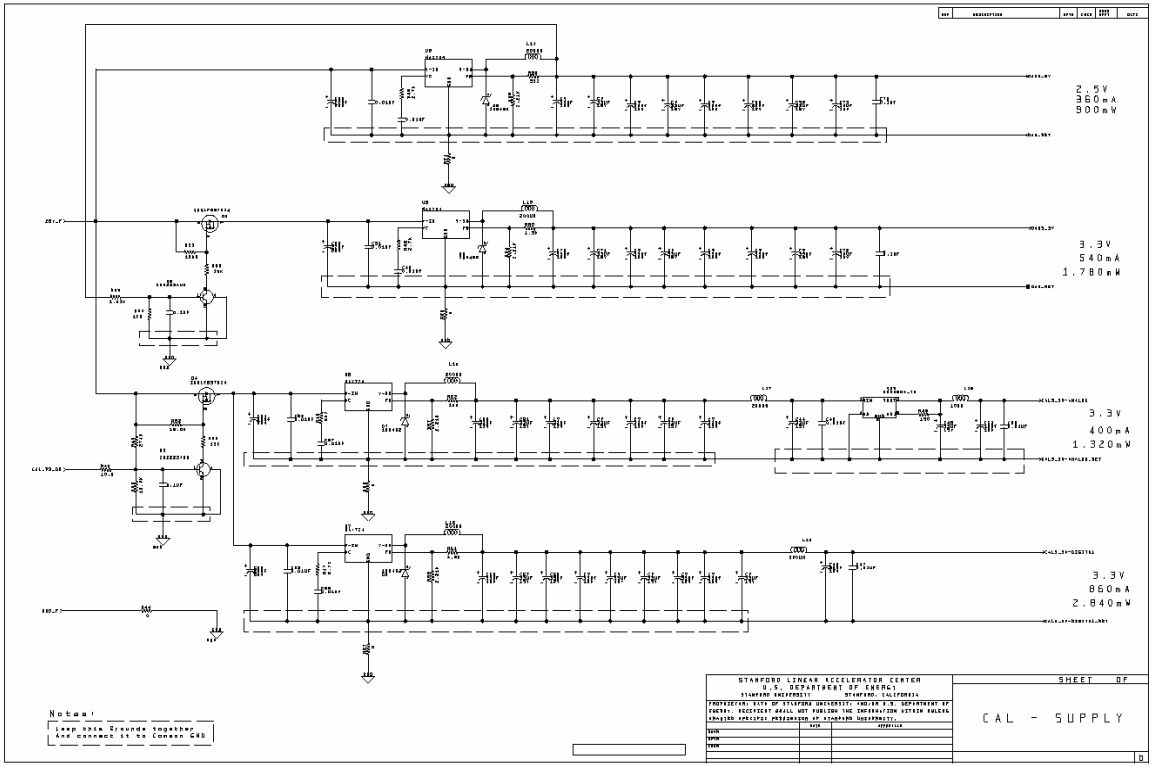
Open Design Issues (TEM Power Supply, 1)

- Input 28V
  - Filtering
  - Inrush current protection
- Output
  - Tem DAQ 2.5V
  - TEM DAQ 3.3V
  - CAL 3.3V Analog
  - CAL 3.3V Digital
  - CAL 0-100V adj
  - TKR 1.5V
  - TKR 2.5V Analog
  - TKR 2.5V Digital
  - TKR 0-150V adj



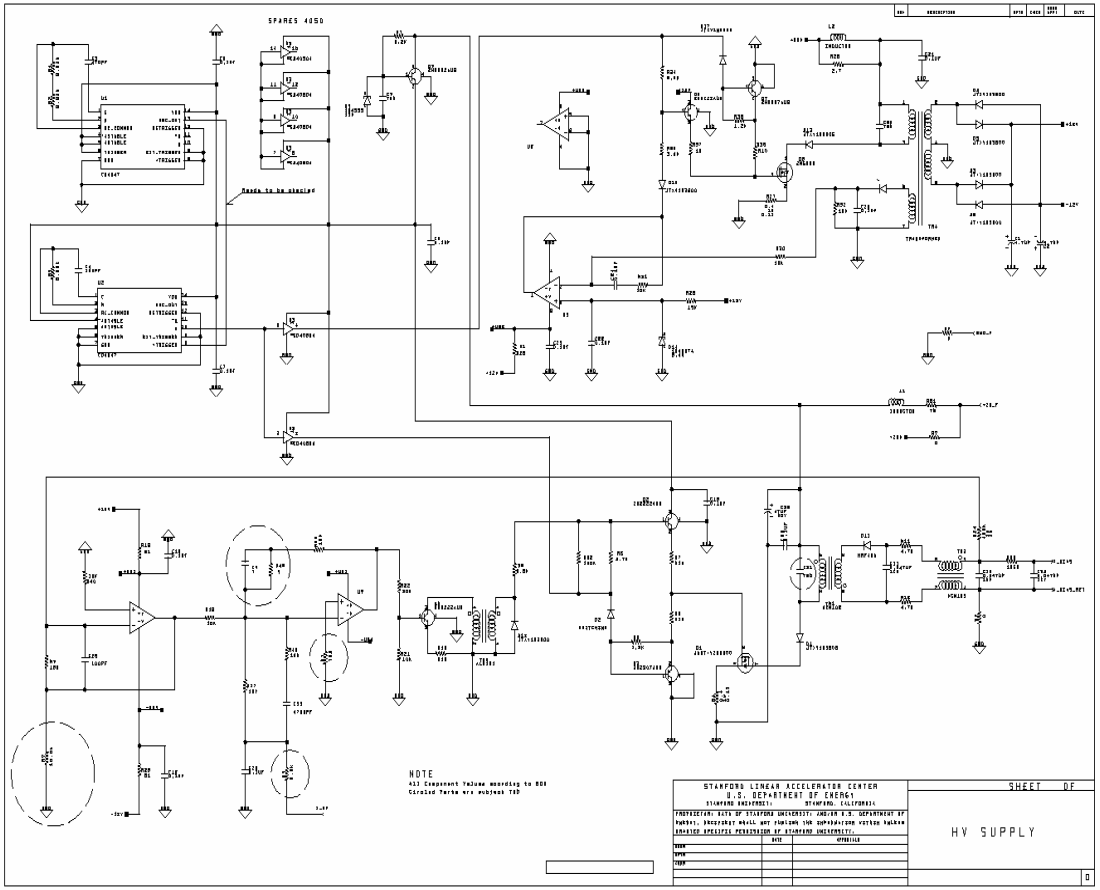
- Overall Schematic finished, working on simulation and layout, details of high-voltage circuit

Open Design Issues (TEM Power Supply, 2)



- Calorimeter and DAQ Low-Voltage (TKR not shown)
  - Uses MAX724 DC/DC regulators
    - No DC isolation, but don't need since spacecraft has DC/DC converters and secondary is LAT side ground

Open Design Issues (TEM Power Supply, 3)



- **High Voltage Supply**
  - **Two circuits being simulated, one from Art Ruitberg, another a slight modification of it. We are working with Art on some modification he is planning to incorporate.**

Parts List

- Almost all parts of DAQ are approved (see Nick's presentation from 7/28/03)
- Most remaining parts need some data from manufacturers, being worked on, plus the ASIC's + Maxim's can only be approved after flight lot is tested

Next 3 Months

- Order all components
- TEM Pre-qual (with ASICs, everything as flight except board-material & non-flight ACTEL's) Used for new EGSE: Oct 1
- Tower Power Supply EM (new design with MAXIM DC/DC converters) Used for new EGSE stands: Oct 1
- GASU EM2 (non-flight memories, FPGA's), Used for ACD multiple FREE test, CAL GSI test: Oct 1
- Finish GASU EM test: Oct 1
- PDU EM (non-flight FPGA): Sept 15
- LAT Comm Board EM (PMC Card). Used for new EGSE stands: Aug 30
- LCB EM (cPCI card) Used for DAQ Internal test-stands: Sept 15
- Storage Interface Board EM (cPCI card) Used for DAQ Internal test-stands: Sept 15
- Crate Backplane EM : Sept 15
- Software EM1 (all SW to completely support TEM-based test-stand including monitoring, plus EM2 filtering, etc): Sept 30
- EGSE TEM (with ASICs) test-stands ready (with EM1 FSW): Oct 1
- Finalize all enclosures (as per PCMS)
- Mini-tower test support

Part Qualification (1)

- **Qualification of DAQ ASIC's**
  - **Following applies to (probable) flight-lot of all 3 (GTCC1, GCCC1, GLTC2)**
    - **SEU: performed at Legnaro last week, engineer will be back this week**
    - **SEL: also tested at Legnaro, but GSFC does not recognize it as sufficient at this time. Thus LAT ASICs will be qualified as family in August at TAMU with TKR MCM**
    - **TID: soon to be done at Legnaro**

Part Qualification (2)

- Function, parametric test plan exists but needs documentation before execution. Not on critical path.
- Based on the parts plan with some tayloring considering parts count for each ASIC.
- Parametric testing: First draft proposal for ACD GARC testing is good but too much for LAT application and no plan to test DAQ, TKR, or CAL ASIC's that way
- Big difference in screening ASIC's
  - For general 3rd party use as opposed to dedicated in-house use on one type of PCB
  - ASIC is on board with very expensive 3rd party components (not true for LAT)
  - ASIC is fabricated in low-yield process (non-commercial)
  - Tasks need to match needs.
  - No added value from experience designing/producing/testing/operating ASICs for many years including knowing likely failure modes
- Instead put additional emphasis to make sure parts work on the board it is supposed to operate over temp, freq, supply level and somewhat less on over-testing the ASIC's.
  - Board test with flight-lot ASICs needs to be done before start of any flight hardware assembly, over T, V, f
- Every ASIC will still be 100% function tested before placement on board
  - Limited performance or parametric testing on 100% of parts
  - Extensive performance and parametric testing on (~5-10) lot samples, just as done for radiation screening.
- In agreement with the plan presented by the Parts Control Board Chairman
  - Same as for TKR ASICs already executed and CAL ASICs
  - LAT Electronics Engineer needs to work with ACD on ASIC test plan before finalizing. LAT Chief EE has not given feed-back yet to ACD. To be done next week.

FSW Comments (1)

- Schedule is in PCMS, but need to work out links before official change control and becoming the baseline
  - Question of efficiency of proceeding with that change control while project is going thru a process which requires modification of sub-system schedules.
  - Two choices:
    - Going ahead with it anyways and spend the time twice
    - Update GSFC monthly on package progress, planned versus actual (e.g did that to project office yesterday)
    - Need decision, either way fine with 4.1.7
- July Status (compare to slide 42, 43 of CDR presentation and PCMS print-out of schedule for change control provided at that time), see next slide

FSW Comments (2)

Package	July Status	To be complete for EM1 release	Comment
GNAT	90%	100%	
GCFG	20%	50%	About 1 week of time
SOP	95%	30%	Way ahead
HSK	0%	50%	Best to put additional manpower on this
MCP	10%	50%	Planned by end of August (take over I&T layer)
SDF	10%	100%	behind
SWD	0	100%	About 5 days of work
LIO	85%	100%	Don't need 100% since CPU-CPU Comm is not needed for EM1
PBS	95%	100%	
PCI	95%	100%	
CCSDS	0%	100%	Trivial, needs a few days

- **Schedule is to provide all FSW needed to run TEM EM1 Model test-stands (single tower)**