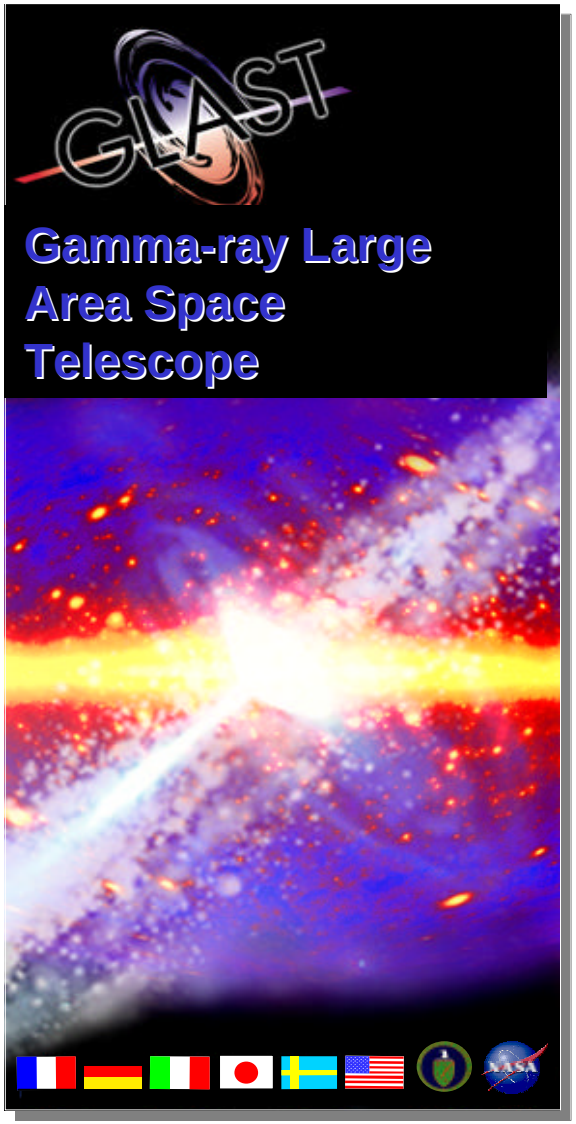

GLAST Large Area Telescope:

Tracker Subsystem
WBS 4.1.4

MRB Update, Round 3
Concerning NCRs 104 and 106

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Reiteration of What We Know

- Within conceivable operational parameter ranges, the issue only concerns readout of mask register contents to the right for GTFE chips at addresses 21, 22, 23 on the MCM.
  - DAC and Mode registers are not affected.
  - Reading the registers to the left is not affected.
  - There is no problem with loading the registers.
  - The problem does not affect readout of SSD strip data.
- The problem is caused by a glitch on the GTFE internal right-hand clock that occurs only when the GTFE chip is driving register contents out onto the MCM single-ended CMOS tri-state bus.
  - This and the hard-RESET are the only signals on the MCM that are single-ended and driven to full CMOS levels (0 to VDD).
  - A large surge of current is necessary to drive the high capacitance of the register read-back bus.
  - Neither MCM single-ended bus is ever active during data acquisition.

Dependencies Already Presented

- Temperature:
  - Lower temperature generally makes the problem worse.
  - Higher temperature is better, as far as this problem is concerned (timing margins are generally worse at higher temperature).
- Voltage
  - At room temperature the problem usually occurs only in a range of voltage somewhat above our operational range (hence it has only been showing up in the –30C test).
- Clock Duty Cycle
  - The problem gets worse for duty cycles somewhat less than 50%.
  - The problem tends to go away for duty cycles somewhat higher than 50% (but this also reduces timing margins for strip data).
- Clock Bus Termination Resistor
  - Within our operational ranges the problem goes away when the termination resistor is reduced from 100 ohms to 75 ohms.

Radiation

- We tried to study the effect of ionizing radiation last week, using the UCSC Co-60 source.
- But the source interlock was jammed, such that we could not raise the Co-60 rods.
- We will try again this week, going to above 10 kRad if possible.
- (Our preliminary guess is that the effect is similar to going to higher temperature.)

More Statistics

- Hiro Tajima tested the 36-MCM setup at SLAC, both before and after changing all the clock-bus termination resistors from 100 ohms to 75 ohms (left and right).
  - 35 MCMs were tested at room temperature with the voltage scanned up to VDD=3.0 V (one MCM was damaged and not used).
  - The internal EGSE clock was used.
  - 17 MCMs did not have mask read-back errors with 100 ohms or 75 ohms.
  - 18 MCMs had errors with 100 ohms *but not with 75 ohms.*
  - (Note that these MCMs have GTRC Version 6 controller chips, which cause some readout problems, but those problems were readily distinguishable from the mask readback issue.)

- An FYI aside: for the 27 MCMs currently in burn-in, only 1 failed the –30C test due to this register readback problem, compared with 9 in the previous set of 27 burned in.

More Statistics

- Marcus Ziegler tested 10 preproduction MCMs (including the 5 reported last time with GTRC V7 and 5 more with GTRC V6) both before and after changing all the clock bus termination resistors from 100 ohms to 75 ohms (left and right).
  - Tested at –20C, 25C, and 60C.
  - Scanned duty cycle from 47% to 53% using an external clock.
  - Frequencies of 20 MHz and 22 MHz.
  - Scanned the voltage from VDD=2.3 V up to 3.0 V for all cases.
  - All 10 show the characteristic mask readback errors to the right with 100 ohm termination in some range of duty cycle, temperature, and voltage.
  - This problem essentially disappears when the resistors are replace by 75 ohms.
    - One board does seem to show the characteristic error at 22 MHz, 48% duty cycle, and –20C (but not at 20 MHz).
    - The boards tend to produce other errors when the margins are pushed, especially at simultaneously high temperature, high frequency, and high duty cycle. These errors involve strip data as well as mask data and look like results of exceeding timing margins. GTRC V6 errors generally are identified with bad parity in the data transmission to the TEM.

More Margins

- SN230 and SN1113 were studied in detail at room temperature with several resistors values: 100Ω, 91Ω, 82Ω, 75Ω, and 43Ω.
  - These have V7 GTRC chips, making data interpretation easier.
  - Duty cycle was varied from 45% to 55% at 20 MHz.
  - The voltage was scanned up to 3.0V in every trial.
- 100Ω:
  - SN230 fails below 52% duty cycle and SN1113 fails below 46%.
- 91Ω:
  - Slight improvement: SN230 fails only below 50% duty cycle at 20 MHz.
- 82Ω:
  - Major improvement: no register readback failures.
- 75Ω:
  - No register readback failures.
- 43Ω:
  - No register readback failures.

Conclusions

- Over a wide range of parameters going well beyond our operational and test ranges, replacing the 100Ω termination by 75Ω cures the register read-back problem that is the subject of NCRs 104 and 106.
  - This is from a sample of 46 MCMs.
  - The only thing we were not able to test yet was radiation dose.
- The change in termination does not introduce any other problems and does not cause any “good” MCMs to go bad.
- Making the same change on the left-hand clock bus does not cause any MCMs to go bad and it does cure the 1 instance seen of a failure to read back the registers to the left (at 48% duty cycle and 22 MHz).
- There is some margin in using 75Ω, as the same result is achieved with 82Ω and with 43Ω.

Recommendations

- Tracker recommendations:
  - Use MCMs as-is for Tower A, providing that
    - They pass all screening in LAT-TD-02367 (including the 3-temperature test). This means that there should be no NCR for the given MCM.
    - And they pass an additional screening at room temperature requiring no register read-back errors for any AVDDB and DVDD between 2.5V and 3.0V.
  - Rework all other existing MCMs to install 75Ω termination resistors on the left and right clock busses.
    - Follow up with the full set of screening tests, but do not repeat the burn-in.
  - Introduce the 75Ω resistor into the Teledyne production asap.