GLAST Large Area Telescope:

Tracker Subsystem
WBS 4.1.4

Tracker ASICs

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Outline

• Introduction/Summary
• System overview
• Requirements
• GTFE designs
• GTFE performance and issues
• GTRC design
• GTRC test results and issues
• Test plan
Summary

• Tracker ASIC tests indicate that the design meets our requirements and goals if a few corrections are made in the production run:
  – Bypass one cell in the GTFE-G to improve yield. The change has been verified by FIB.
  – Fix logic errors in the GTRC3 related to TOT and parity reporting.
  – Improve timing margin by changing the GTRC clock edge for receiving GTFE data (or raise DVDD, or lower frequency).
• To hold the LAT schedule, the ASIC production must go out now (critical path leading to the Tracker qualification unit).
• To guarantee that we do not come up empty handed 4 months from now, when the ASICs are needed, we must have a backup plan consisting of submission of existing, unmodified designs. In the worst case this means
  – No reliable TOT information (not a science requirement).
  – Incomplete reporting of possible bit errors.
  – Higher power (by about 30W).
  – Possible calibration complications due to GTFE-F2 comparator behavior.
Failsafe/redundancy scheme:
- Serial, LVDS readout and control lines.
- Two readout and control paths for every 64-channel front-end chip.
- Any single chip can fail without preventing the readout of any other.
- Either of the two communications cables can fail without affecting the other.

- Trigger output = OR of all channels in a layer.
- Upon trigger (6-fold coincidence) data are latched into a 4-event-deep buffer in each front-end chip.
- Read command moves data into 1 of 2 GTRC buffers.
- Token moves data from GTRCs to TEM.
TMCM (Readout Module)

- 8-layer polyimide PWB
- Top edge thickened and machined to a 0.64 mm radius
- 1-layer flex circuit ("pitch adapter") bonded over the radius
- 24 64-channel GTFE chips
- 2 GTRC chips
- 2 nano connectors
- SMT parts
- Steel mounting screws + transfer adhesive

Diagram:
- Machined corner radius with flex circuit bonded around the curve
- TMCM, attached by screws
- High-thermal conductivity transfer adhesive
- Tray Structure
- Bias circuit
- Readout IC
- Detector
- Grounding Screws, 3 Total
- Mounting Screws, 1 of 8
- Connector, 1 of 2
- GTRC, 1 of 2
- GTFE, 1 of 24

Dimensions:
- 359.0mm
- 24.58mm
- 18.0mm
TKR Electronics Requirements

• Details of the requirements are in
  – LAT-SS-17 Performance requirements
  – LAT-SS-134 Mechanical & Thermal requirements
  – LAT-SS-152 Electronics requirements

• The major challenges are
  – Low power: <168 W of conditioned power
    • Less than 0.29 W per TMCM or 190 µW/channel
  – Low noise occupancy: (noise trigger rate <500 Hz)
    • The trigger requires occupancy less than 5/100,000 ch/trigger
    • Readout and onboard processing requires <1/10,000 ch/trigger
  – Compact packaging: bring signals around the tray corner
  – Manufacturing and QC: 884,736 channels in outer space
  – Reliability: design, testing, redundancy
Some Detailed Requirements

- Internal charge injection for calibration and test, with a DAC to control the pulse height and a mask to select any set of channels.
- Threshold uniformity: <15 mV rms across 64 channels.
- Threshold control per GTFE chip by an internal DAC.
- Readout speed & dead time: less than 10% at 10 kHz cosmic rate.
- TOT: measure up to 4 MIPs.
- Non-destructive readback of configuration registers.
- 2-bit word sent with the trigger and returned by the GTFE chip, to ensure that events are never mixed up unknowingly.
- Layer-OR jitter $\pm 250$ ns for a charge deposit $>0.5$ MIP.
- Reliability:
  - Redundant readout paths.
  - Redundant power paths.
  - Protection against power shorts.
- Radiation hardness; 4 kRad TID; $>37$ MeV/mg/cm$^2$ SEL thresh.
- Passive cooling; temperature monitoring.
## Tracker Electronics Documents

<table>
<thead>
<tr>
<th>Document Code</th>
<th>Description</th>
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<tr>
<td>LAT-SS-152</td>
<td>Tracker Subsystem Level-IV Electronics Specification</td>
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<td>Tracker Electrical Interface Specification</td>
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<td>Tracker Readout Electronics Conceptual Design</td>
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<td>LAT-TD-173</td>
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<td>LAT-SS-1116</td>
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<td>Tracker Front-end Readout ASIC Prototype Test Plan</td>
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<td>LAT-TD-153</td>
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<td>LAT-TD-191</td>
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## Tracker Electronics Documents

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<td>Tracker Front-end Readout ASIC Wafer Test Procedure</td>
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<tr>
<td>LAT-TD-248</td>
<td>Tracker Readout Controller ASIC Wafer Test Procedure</td>
</tr>
<tr>
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<td>Tracker Multi-Chip Module Test Plan</td>
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<tr>
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</tr>
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<td>LAT-TD-179</td>
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</tr>
</tbody>
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F.E. Readout Chip (GTFE)

- Schematics-based design, using standard cells for logic.
- Manual layout of the analog channel, I/O cells, memory, global routing.
- Automated place-and-route of the logic blocks.
- Two versions under test:
  - F2 (AC coupling from shaper to comparator)
  - G (DC coupling from shaper to comparator)
• 64 amplifier-discriminator channels
• 7-bit threshold DAC
• Calibration mask register
• 7-bit calibration DAC
• Trigger mask register and trigger layer-OR
• Data mask register
• 4-deep event buffer
• Pair of redundant command decoders
• Pair of redundant trigger receivers
• Leftward readout register
• Rightward readout register
• LVDS I/O cells
F2 Version Shaper

No source-follower stage

1 per 64 channels
G-Version Shaper

1 per 64 channels

"Threshold Conditioner" Cell
Readout Controller Chip (GTRC3)

- All digital
- Tanner standard-cells, except for
  - LVDS I/O cells.
  - SEU hardened configuration register.
  - RAM (64 hits, 2 buffers)
- Design in VHDL; synthesis, auto place and route.
Tracker ASIC Test Program

- Padova group (R. Rando, et al.): radiation testing.
- Relevant test plans for today’s results:
  - LAT-TD-153, Tracker electronics test plan
  - LAT-TD-881, test plan for the preproduction ASICs
  - LAT-TD-246, GTFE prototype test plan
  - LAT-TD-247, GTFE wafer test procedure
  - LAT-TD-248, GTRC wafer test procedure
  - LAT-TD-249, MCM test plan
  - LAT-TD-1059, radiation test plan
GTFE Wafer Testing

- 17 wafers with 45 chips of each type were probed.
- A complete set of test vectors was executed, and threshold scans were made.
- All digital functionality was checked, except for I/O on the chip-to-chip connections (due to problems with the probe card).
- The yield was excellent, except for about 15% of the G chips that have a threshold instability (more on this later).

<table>
<thead>
<tr>
<th></th>
<th>GTFE Version-F2</th>
<th>GTFE Version-G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield for digital tests 201 through 207.</td>
<td>95.5%</td>
<td>94.5%</td>
</tr>
<tr>
<td>Yield including threshold scan test.</td>
<td>94.8%</td>
<td>79.8%</td>
</tr>
</tbody>
</table>
Threshold Scans (Ladder + mini-MCM)

Channel C241

Mean = 40.17
Sigma = 5.78

G chip channel

Channel C286

Mean = 33.16
Sigma = 6.82

F2 chip channel
Threshold Scans

- 3 full-length ladders with mini-MCMs have been tested:
  - Hold the charge injection constant and scan the threshold
  - Hold the threshold constant and scan the charge injection

![Gain vs ENC graph]

This is for about 1.6 fC charge injection. The gain is nonlinear.
### Threshold Scans

<table>
<thead>
<tr>
<th>LDR</th>
<th>Chip</th>
<th>Type</th>
<th># Ch</th>
<th>Gain (mV/fC)</th>
<th>Std Dev</th>
<th>ENC (elec)</th>
<th>Std Dev</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0</td>
<td>G</td>
<td>63</td>
<td>94.3</td>
<td>6.8%</td>
<td>1657</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>G</td>
<td>64</td>
<td>126.4</td>
<td>5.0%</td>
<td>1361</td>
<td>120</td>
</tr>
<tr>
<td>80V</td>
<td>2</td>
<td>G</td>
<td>63</td>
<td>114.7</td>
<td>5.6%</td>
<td>1424</td>
<td>145</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>G</td>
<td>61</td>
<td>123.4</td>
<td>3.9%</td>
<td>1267</td>
<td>103</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>F2</td>
<td>62</td>
<td>93.0</td>
<td>8.2%</td>
<td>2008</td>
<td>201</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>F2</td>
<td>61</td>
<td>88.3</td>
<td>6.4%</td>
<td>2011</td>
<td>289</td>
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<tr>
<td>11</td>
<td>0</td>
<td>F2</td>
<td>62</td>
<td>90.1</td>
<td>5.5%</td>
<td>2102</td>
<td>156</td>
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<tr>
<td></td>
<td>1</td>
<td>F2</td>
<td>60</td>
<td>68.7</td>
<td>6.6%</td>
<td>2159</td>
<td>227</td>
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<tr>
<td>110V</td>
<td>2</td>
<td>F2</td>
<td>59</td>
<td>66.8</td>
<td>7.6%</td>
<td>2220</td>
<td>312</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>G</td>
<td>64</td>
<td>106.9</td>
<td>7.2%</td>
<td>1367</td>
<td>149</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>G</td>
<td>64</td>
<td>93.3</td>
<td>8.1%</td>
<td>1449</td>
<td>189</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>G</td>
<td>64</td>
<td>103.3</td>
<td>6.9%</td>
<td>1454</td>
<td>171</td>
</tr>
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</table>

The charge injected was about 1.6 fC.
## Charge-Injection Scan (THR=22)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Type</th>
<th># Ch</th>
<th>Q (fC)</th>
<th>Gain (mV/fC)</th>
<th>Std Dev</th>
<th>ENC (elec)</th>
<th>Std Dev</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>F2</td>
<td>64</td>
<td>1.27</td>
<td>83.6</td>
<td>5.9%</td>
<td>2119</td>
<td>132</td>
</tr>
<tr>
<td>1</td>
<td>F2</td>
<td>64</td>
<td>1.57</td>
<td>67.3</td>
<td>5.8%</td>
<td>2048</td>
<td>107</td>
</tr>
<tr>
<td>2</td>
<td>F2</td>
<td>64</td>
<td>1.63</td>
<td>65.1</td>
<td>6.8%</td>
<td>1962</td>
<td>278</td>
</tr>
<tr>
<td>3</td>
<td>G</td>
<td>64</td>
<td>1.10</td>
<td>97.0</td>
<td>5.6%</td>
<td>1436</td>
<td>99</td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>64</td>
<td>1.20</td>
<td>88.5</td>
<td>7.2%</td>
<td>1578</td>
<td>148</td>
</tr>
<tr>
<td>5</td>
<td>G</td>
<td>64</td>
<td>1.10</td>
<td>96.5</td>
<td>4.4%</td>
<td>1530</td>
<td>96</td>
</tr>
</tbody>
</table>
Problem with Last 2 Channels of F2

Channels 62 & 63 on 3 F2 Chips

Hypothesis: feedback from comparator to shaper via a test pad that exists only on each of these two channels. (Double-pulses are seen on an oscilloscope.)
Simultaneous Multiple Channels

G Chip, 8 Channels Pulsed Simultaneously

32 Channels Pulsed Simultaneously

No load on the amplifier inputs.
F2 Version

Note: the noise measurements presented above were made by simultaneously pulsing 8 channels per chip.

No load on the amplifier inputs.
G-Version Unstable Chips

• About 15% of the G-version chips show oscillations on the Layer-OR output with the threshold set to >5 DAC counts (about 0.24 fC), with some still oscillating at threshold >30 DAC counts.

• The problem was isolated to the “threshold conditioner” cell. Good chips could be made bad and vice-versa by adjusting the bias of the output driver of this cell (using a probe on internal test pads).

• 8 of the worst oscillating chips were modified by FIB to bypass this cell, and they all behaved normally afterwards on mini-MCMs. So far one was connected to a ladder and had excellent noise scans. (One more FIB chip was damaged and is completely dead.)

• Spice simulations show that the impedance of the threshold bus is greatly reduced and the amount of “kick-back” from the comparator is reduced by more than 10 when this cell is removed.

• 24 “good” chips were selected by the wafer-probing data and tested on a full-size MCM. All behaved well on the MCM, including over the temperature range –30C to +50C.
G-Version Shaper

1 per 64 channels
G-Version FIB Edit

Add via M1 to M2 to M3 (692, 11188)

Cut M1 trace (750, 11187) Add via M1 to M3 (753, 11187)

Remove M2 to M3 via (753, 11136)
All 64 channels in just one chip were enabled, and the Layer-OR rate was measured by a frequency counter for each threshold setting. For ladder 0:

Trigger Rate per Chip (64 Channels)

1.3 fC=1/4 MIP

Long TOT pulses; look like cosmic rays
Noise Occupancy

Measured on 2 ladders so far. About $10^{-6}$ per trigger.

Ladder 0, 80V bias, 1.3 fC threshold, 1.5 million triggers.
Effect of Readout on Noise

- Ladder 11, biased at 110V.
- Set thresholds at 1.3 fC (using gains measured in the calibration charge-injection scan).
- Load a hit pattern into the GTFE memory by charge injection (every 8\textsuperscript{th} channel hit; other patterns will be investigated).
- Monitor the Layer-OR with all 384 channels enabled.
- Execute a test vector involving a complete readout sequence, and count how many pulses appear on the Layer-OR during execution of the vector. Repeat 1000 times.
- Execute a test vector involving only a clock (no commands) and count the Layer-OR pulses. Repeat 1000 times.

- Layer-OR rate with clock only (no readout): 448 Hz. \textbf{No effect.}
- Layer-OR rate with readout: 440 Hz.
Measure the Layer-OR width with internal (both ranges) and external charge injection into a single channel.

Time Over Threshold, GTFE-G

- External Injection
- Internal, Low Range
- Internal, High Range
- Spice Simulation

Timing out the counter at 50 $\mu$s gives a range of about 5.2 MIPs.

Evidence of some problem with our DAC calibration measurements.
The TOT saturates at about 150 µs when the preamp saturates.

Time Over Threshold, GTFE-G

- **External Injection**
- **Internal, Low Range**
- **Internal, High Range**
- **Spice Simulation**

VDD=2.5 V
Example Shaper Waveforms

GTFE64G FIB, Channel 2

- Cal DAC=8
- Cal DAC=26
- Spice, 14 mV
- Spice, 42 mV

V (mV)

0 5 10 15 20

t (microseconds)
Example Shaper Waveforms

F2 Chip Shaper Output; No Input Load

CAL-DAC=30
CAL-DAC=20

Comparator transition
# MCM Power Measurement

<table>
<thead>
<tr>
<th>Condition</th>
<th>AVDDA 1.5 V</th>
<th>AVDDB 2.5 V</th>
<th>DVDD 2.5 V address 5</th>
<th>DVDD 2.5 V address 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Clock, G</td>
<td>77.4 mW</td>
<td>39.3 mW</td>
<td>134.3 mW</td>
<td>82.8 mW</td>
</tr>
<tr>
<td>20 MHz, G</td>
<td>77.4 mW</td>
<td>39.3 mW</td>
<td>134.3 mW</td>
<td>138.5 mW</td>
</tr>
<tr>
<td>20 MHz, F2</td>
<td>77.4 mW</td>
<td>28.0 mW</td>
<td>134.3 mW</td>
<td>138.5 mW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition</th>
<th>F2 (W)</th>
<th>G (W)</th>
<th>Allocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCM Address &gt; 0</td>
<td>0.240</td>
<td>0.251</td>
<td></td>
</tr>
<tr>
<td>MCM Address = 0</td>
<td>0.244</td>
<td>0.255</td>
<td></td>
</tr>
<tr>
<td>Tower</td>
<td>8.66</td>
<td>9.05</td>
<td>10.5 W</td>
</tr>
<tr>
<td>16 Towers</td>
<td>139</td>
<td>145</td>
<td>168 W</td>
</tr>
</tbody>
</table>
**DAC Calibration**

**CAL-DAC**

**THR-DAC**

Threshold DAC at VDD=2.5V

- Intercept = 7.37 mV
- Slope = 4.94 mV

Threshold DAC Calibration at VDD=2.5

- Intercept: 9.53 mV
- Slope: 10.1 mV

**Tracker, WBS 4.1.4**
### DAC Calibration

- Except for current-mirror errors, the intercept should be equal to the slope.
- Deviation from this expectation as well as the Spice prediction casts some uncertainty on the measurements.

<table>
<thead>
<tr>
<th>Range</th>
<th>Intercept Measured</th>
<th>Intercept Predicted</th>
<th>Slope Measured</th>
<th>Slope Predicted</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cal Low</td>
<td>2.01 mV</td>
<td>1.57 mV</td>
<td>1.43 mV/cnt</td>
<td>1.53 mV/cnt</td>
</tr>
<tr>
<td>Cal High</td>
<td>14.3 mV</td>
<td>15.0 mV</td>
<td>11.4 mV/cnt</td>
<td>14.6 mV/cnt</td>
</tr>
<tr>
<td>Threshold Low</td>
<td>7.37 mV</td>
<td>4.5 mV</td>
<td>4.94 mV/cnt</td>
<td>4.5 mV/cnt</td>
</tr>
<tr>
<td>Threshold High</td>
<td>9.53 mV</td>
<td>12.9 mV</td>
<td>10.1 mV/cnt</td>
<td>12.9 mV/cnt</td>
</tr>
</tbody>
</table>
GTRC & MCM Testing

- The GTRC3 chip has been found to have these logic bugs:
  a) The TOT measurement is not buffered properly and will not stay aligned with the hit data at high rates.
  b) The parity is not calculated correctly for data read out from the right hand side.
  c) Parity errors in the commanding are not reported properly.
- These bugs have been understood and fixed in the VHDL.
- Bugs (a) and (b) were quickly found and fixed in the GTRC5 submission, due to be received in a few days.
- All bug fixes and the following modifications are being prepared for the GTRC6 submission:
  - Latch data from the GTFEs on the falling clock edge, to improve the timing margin.
  - Remove the data field from data-less commands.
- The revised VHDL is under test in an FPGA version of the GTRC, working on boards with actual GTFE chips.
# Timing/Voltage Margins

<table>
<thead>
<tr>
<th>DVDD (V)</th>
<th>Clock (MHz)</th>
<th>GTFE Data</th>
<th>GTFE Ctrl Reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>10</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>NG</td>
<td>NG</td>
</tr>
<tr>
<td>2.6</td>
<td>20</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>22</td>
<td>OK</td>
<td>NG</td>
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<td>NG</td>
<td>NG</td>
</tr>
<tr>
<td>2.9</td>
<td>25</td>
<td>OK</td>
<td>OK</td>
</tr>
</tbody>
</table>

Measured on a full-scale MCM (24 GTFE chips), but with the clock/cmd bus termination resistors still at the wrong end.
The GTFE internal delays are double the Spice prediction until all extracted trace parasitics are included. Then we get good agreement. The overall delay could be reduced by increasing the size of several drivers and/or by realigning the data with the clock immediately before the GTFE output driver.

### Components of the Round-trip Delay

<table>
<thead>
<tr>
<th>GTFE internal; measured on test pads.</th>
<th>Components of the Round-trip Delay</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 V</td>
<td>Driving the MCM clock bus from the GTRC</td>
<td>~10</td>
</tr>
<tr>
<td></td>
<td>Receiving the clock into the GTFE</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>Delay of GTFE internal control logic in getting the clock to the read register.</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Delay in establishing the DAC output onto the long internal GTFE trace.</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>Delay in getting the signal to the GTFE output pad</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Delay in charging up the MCM bus and receiving the bit into the GTRC</td>
<td>~10</td>
</tr>
</tbody>
</table>

Total is nearly 50 ns!
The GTFE delays by about $\frac{1}{2}$ clock cycle, as shown above.

Delays sending the clock out of the GTRC and receiving the differential data into the GTRC account for most of another $\frac{1}{2}$ cycle, leaving little margin at 2.5V.
Solutions to the Timing Problem

Select one of the choices below:

1. Increase the operating voltage to 2.9 V for AVDDB and DVDD.
   • MCM power increases by ~52 mW. LAT power increases by about 30W, putting the Tracker 7W over allocation.

2. Lower the system clock to 18 MHz.

3. Lower the Tracker clock to 10 MHz, keeping the system at 20 MHz.

4. Latch the data into the GTRC on the falling clock edge.
   • Depends on the fact that the delays now put the data edge very close to the GTRC clock rising edge.
   • We would be in trouble if the delays changed in the next run to much shorter values. Unlikely, but we put in a programming wire-bond pad to revert to the clock rising edge (GTRC6).
   • If the system is run on a slow clock, then the data get latched a clock cycle early. GTRC has to be reprogrammed to adjust.
   • There will probably be a small frequency range <<20 MHz where the system cannot be adjusted to read properly both registers and data without programming the GTRC in between.
Misc. Other Tests

• GTRC LVDS levels (address=0 and address ≠ 0).
• Detailed measurements on GTFE I/O cells (LAT-TD-545).
• Radiation testing at LNL (Italy) on a mini-MCM.
  – Only the GTRC was tested so far.
  – 5 ions from Si to Au.
  – TID of 30 kRad. GTRC still operated at 20 MHz.
  – No latch-up, even at LET=82 MeV/mg/cm².
  – SEU rate in the configuration register was consistent with the earlier test chip (LAT-TD-333).
Electronics Test Planning

• Before GTRC submission:
  – Complete check-out of the GTRC6 VHDL on the 3 test boards, each with 2 GTRC-FPGAs and 2 GTFEs.

• ASAP:
  – Complete and test the FPGA test board with 24 GTFEs.
  – Tests with high-rate readout and random trigger:
    • High-rate test of a ladder/mini-MCM using a beta source.
    • Self trigger at high rate on noise in one or a few channels, both on a mini-MCM and the FPGA board.
  – Connect the mini-MCM loaded with FIB G chips to a ladder and test.

• EM MCM production at Teledyne: starting next week test boards coming off of their production line (LAT-TD-249).
Electronics Test Planning

- 6 EM MCMs to be delivered to the electronics group for their own tests.
- 2 EM MCMs for environmental testing at UCSC and SLAC.
- 8 MCMs on functional engineering-model trays.
  - One tray for environmental testing in Italy.
  - Four trays (6 MCMs) for mini-tower testing at SLAC.
    - First cosmic-ray tests since the BTEM tower.
    - Develop and execute tower-level test code (LAT-TD-191).
- Production wafer testing:
  - Redo and improve the GTFE probe card and test system.
  - Redo and test on existing wafer the GTRC probe card.
  - M. Ziegler working with D. Marsh to bring the UCSC wafer-probing area into compliance (contamination control, etc.).
  - Work in progress to incorporate this into the database.
Conclusion

Tracker ASIC Fabrication Proposal

• Details still need to be agreed upon following and depending upon the conclusion of this review.

• Front-end ASIC
  – Submit the GTFE-G2 (G version with “threshold conditioner” removed). The layout is verified and ready.
  – Backup with the GTFE-F2 (no changes). Begin a study of the operational implications of its performance, to be prepared.

• Readout Controller ASIC
  – Submit the GTRC6, after completion of verification in the FPGAs.
  – Backup with the GTRC3 (no changes) and the GTRC5. No cost impact of this. We will have the GTRC5 prototype very soon to test.
  – Study further implications of having to use the GTRC3.