GLAST Large Area Telescope:

Tracker Subsystem
WBS 4.1.4

GTRC Timing & TOT Issues
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GTRC V6 Design Problems

- GTRC Time Over Threshold:
  - Logic in existing chip is flawed (causes frequent DAQ time-outs) and can only be repaired by repeating the production. Existing chip can only be used with the time-over-threshold disabled.
  - The problem occurs when a second trigger is received in coincidence with the falling edge of the time-over-threshold.
  - The TOT algorithm can be done in the TEM ASIC. This will soon be tested in the FPGAs of an EM TEM.

- GTRC data input bias:
  - Recently discovered that some MCMs don’t like to be at the top of the readout chain.
  - We then realized that the GTRC wafer test did not verify the self biasing of the data inputs.
  - We will fix this by adding two resistors to the flex-circuit cables to bias those inputs (to logic zero) externally. Not a problem. This will be more safe than relying on the internal bias.
GTRC V6 Design Problems

• GTRC to GTRC data transfer and timing margins:
  – Observed internal delays are now understood in simulation.
  – Big margins at 20 MHz can be achieved by redesigning the GTRC to output data on the rising clock edge, but schedule...
  – Using the existing chips:
    • At 20 MHz and 2.5V they skip a clock on each transfer.
      – Not a problem in itself (same timing as would be achieved by output on the rising edge), BUT
        » Fails if the frequency is lowered to 19 MHz.
        » Fails at 20 MHz if the voltage is raised.
    • It works properly up to about 15 MHz at 2.44V, or to higher frequency if the voltage is raised (but insufficient power to fix the problem).
    • The frequency limit of correct operation can be raised a little by lowering the termination resistance, with 200-ohm external resistors placed in parallel with the existing internal 700 ohms.
      – Requires 16 resistors on each flex-circuit cable (not difficult or expensive).
      – Still cannot achieve 20 MHz with good margins.
GTRC Data Transmission

Measured ~28 ns delay from A to B is well understood now.
• Measurements made on a string of 9 MCMs (i.e. one tower side) connected to a TEM via burn-in flex-circuit cables, using connectors savers.

• No additional termination resistors have been added to the system.

• The voltages listed here are measured at the chips. The voltage at the TEM is higher.
The Agilent process is designed for maximum 3.3V operation. This slide shows the margins with the maximum voltage we can achieve with our existing TEM/PS. Probably the margin will continue to increase if we push up to 3.3V.
GTRC V6 with 200-ohm Termination

- Adding 200 ohms in parallel with the existing 700 ohm termination speeds up the rise time of the signal on the cable between GTRC chips and raises a little the maximum operational frequency.
- We have not yet finished the complete survey of this condition because the TEM broke during the measurements.
- Safe operation could be achieved at about 16 MHz with the voltage at the TEM raised from 2.5 V to 2.75 V.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>2.45 V at TEM</th>
<th>2.61 V at TEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°C</td>
<td>15.8 MHz</td>
<td></td>
</tr>
<tr>
<td>30°C</td>
<td>15.8 MHz</td>
<td></td>
</tr>
<tr>
<td>35°C</td>
<td>15.6 MHz</td>
<td>17.2 MHz</td>
</tr>
<tr>
<td>40°C</td>
<td>15.4 MHz</td>
<td></td>
</tr>
<tr>
<td>45°C</td>
<td>15.3 MHz</td>
<td>16.0 MHz</td>
</tr>
<tr>
<td>50°C</td>
<td>15.1 MHz</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage at TEM</th>
<th>Maximum freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.46</td>
<td>15.5 MHz</td>
</tr>
<tr>
<td>2.61</td>
<td>17.0 MHz</td>
</tr>
<tr>
<td>2.76</td>
<td>18.5 MHz</td>
</tr>
<tr>
<td>2.93</td>
<td>19.6 MHz</td>
</tr>
<tr>
<td>3.00</td>
<td>20.2 MHz</td>
</tr>
<tr>
<td>3.08</td>
<td>20.6 MHz</td>
</tr>
</tbody>
</table>
Test of FIB Patched GTRC

- Layout was modified by ion beam to send data and token out on the rising clock edge.
- These scope traces show transmission of register readback data.
Test of FIB Patched GTRC

20 MHz

GTRC-1 Data Out

GTRC-0 Data Out

Clock In

21 Oct 2003
15:05:03
Test of FIB Patched GTRC

- Three of the patched GTRC chips were operated on separate MCMs and read out in a chain using burn-in cables with connector savers.
- Only done at room temperature so far, but margins are large enough that we don’t expect to see an issue with temperature. (Doing test from –20°C to +60°C today.)
- All frequencies above 5 MHz were tested (in 0.1 MHz steps).
- Both register readback and data (charge injection) are tested.
- The upper frequency limit is consistent with the internal limitations of the MCMs. (We have also tested MCMs stand-alone from 1 MHz to this upper limit.)

<table>
<thead>
<tr>
<th>Voltage on MCM at Chips</th>
<th>Maximum Frequency of Proper Operation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.29 V</td>
<td>25 MHz</td>
</tr>
<tr>
<td>2.56 V</td>
<td>27 MHz</td>
</tr>
<tr>
<td>2.84 V</td>
<td>29 MHz</td>
</tr>
</tbody>
</table>
Test of V7 VHDL Code

- We have installed the updated VHDL code into 3 FPGA test boards. Each test board has 2 FPGAs, which play the GTRC role, and 2 GTFE amplifier chips.

- Two FPGA test boards are being operated with the TEM system, and no problems have been seen so far with reading back registers and charge-injection “data”.

- The third FPGA test board was modified to be operated directly from a COM card (VME I/O card), with the GTFE chips disconnected. This allows us to input fake “GTFE data” into the GTRC FPGA directly from the VME. In this way we can execute the complete set of GTRC wafer test vectors (see LAT-TD-00248) through the new VHDL code. Preliminary results from last night (will verify today):
  - No problems seen in execution of the test vectors.
  - The TOT problem seen in V6 chips does not show up in this test.
Schedule Impacts

- It should be possible to submit the V7 design next week.
- These productions have been taking 8 to 9 weeks at MOSIS.
- The received wafers can be probed and diced in a week.
- Complete check-out of V7 will require tests on MCMs and trays, so volume production of MCMs would proceed at risk (small risk, I believe).
- The MCM preproduction will begin next week with V6 chips.
- The new GTRC V7 chips could be available by late January, which would represent 2 or 3 weeks delay in the start of flight MCM production (i.e. for tower A).
- We will design pads into the flex-circuit cables for termination and bias resistors, even though they may not be used in the end.
Conclusions

• The design problems and their origin are well understood.
• Using the existing GTRC V6 chip in the full LAT is only possible if
  – The TOT algorithm is disabled in the GTRC (it could be recovered by making a new TEM ASIC).
  – The entire LAT operates at no higher than about 16 MHz (with termination resistors added to the cables). Even this does not have a highly comfortable margin.
  – See the following plots for background information on the frequency impact on the Tracker triggering, the impact of voltage on Tracker power, and the importance of the TOT to the science performance.
• With just a single tower equipped with GTRC V6, the full LAT could operate at a higher frequency (maybe 18 MHz) by running the V6 tower at higher voltage (requires a special TEM/PS for that tower).
• We know how to fix the design to correct both the TOT and the timing margins:
  – New logic code verified in FPGAs as well as simulation.
  – New timing verified by FIB patching of existing chips.
Mini-Tower Hit Efficiency

From Hiro Tajima, measured using cosmic rays under 3 different trigger conditions. 5 layers are used for tracking (exactly 5 clusters required, with straight track in the view with 3 hits); the 6th layer is used to find the hit efficiency, including cutting away from dead areas between wafers.

- External Trigger: Zero on this scale is about 0.9 \(\mu s\) after passage of the particle.
- Tracker Trigger: The peak amplifier pulse height occurs at about 1.0 to 1.5 \(\mu s\) TACK delay.
- CAL Trigger: For the EXT trigger (scintillator), zero on this scale is about 0.9\(\mu s\) after passage of the particle.
• Measurements made this week at 20 MHz with the latest MCMs.
• Assuming 4 µA/SSD at 120 V bias (total of 4.4 W of bias power).
• CDR allocation: 155 W.
TOT Analysis (Simulation)

TOT Asymmetry between 1\textsuperscript{st} 3 and last 3 planes.

100 MeV Gammas

Albedo Protons

TOT Average

TOT here is truncated to 250 counts by GTRC
TOT Analysis (Simulation)

The asymmetry is not useful with the 50 microsecond truncation imposed in the GTRC design.

But the average TOT still gives good separation, only about 10% worse than with no truncation.
Background Analysis (Simulation)

3 Classes of Background Events Remain:
- Range-outs from below (.04 Hz)
- Horizontal Events (.004 Hz)
- ACD Leakage and inefficiency (.04 Hz)

Elimination Strategy

1) Range-outs
   - ToT Identification in Tracker - kills > 90%
   - MIP Identification in CAL - should kill > 50%

2) Horizontal Events - should kill > 50%
   - Edge CAL hits

3) ACD Leakage
   - Events found accurately;
   - Cover cracks with Tapes - should kill > 95%

Estimated Rate after this to be < .006 Hz
   (about 3% residual background in EGD signal)

$A_{\text{eff}}$ & Background Rate:
$A_{\text{eff}} = 8400 \text{ cm}^2$ on Axis ($E > 3 \text{ GeV}$)
$A_{\text{eff}} \times \Delta\Omega = 2.0 \text{ m}^2\text{-str}$

BUT....
Background Rate 4-5 times too high

Analysis of 25M MC Mixed BKG Events
(Bill Atwood)