ASIC Design Flow for e.g TKR Controller

- VHDL
- Simulation
- Netlist
  - Manual: Schematic of IO, LVDS
  - Automatic: Generate Schematic
- Automatic: Layout, Place&Route
  - Layout: Add IO and LVDS, Result: Complete Chip Layout
- Compare
- Full-Chip Compare
  - Simulation: Spice
  - Full Chip Schematic
- Simulation: Full Chip Schematic
- Netlist
  - Netlist w/o Parasitics
  - Netlist with Parasitics
- Full-Chip Simulation with Synopsys
- Full-Chip Simulation with Synopsys