Production and Test of Front-End Electronics for the GLAST LAT Silicon Tracker

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Abstract

The Gamma-ray Large Area Space Telescope (GLAST) is an astronomical satellite mission to explore the gamma-ray universe from low earth orbit, scheduled to be launched in 2007. The Large Area Telescope (LAT) on board GLAST detects gamma-rays by the pair-conversion process, using a silicon tracker-converter and a CsI calorimeter. A total of 880,000 strip signals on about 80 square meters of silicon are processed by the readout electronics. Two custom ASICs, the front-end readout chip (GTFE) and the readout controller chip (GTRC), are used in a front-end electronics module to meet the severe requirements for this space application. In this paper, production of the front-end electronics for flight units and their test results are described.

Key words: gamma-ray, space application, pair-conversion, silicon strip, tracker
PACS:

1 Introduction – Overview of the GLAST Silicon Tracker

The Gamma-ray Large Area Space Telescope (GLAST) [1][2] is designed to follow the greatly successful mission of the EGRET instrument on-board the Compton Gamma-Ray Observatory. EGRET was the first instrument with the effective area and background rejection system necessary to detect a large number of galactic and extragalactic gamma-ray sources and thus extended the field of gamma-ray astronomy [3]. The GLAST mission will carry two instruments: the Large Area Telescope (LAT) and the Gamma-ray Burst Monitor (GBM). The LAT is designed to improve upon the sensitivity of EGRET by a factor of 30 at 100 MeV and by even more at higher energies, including the largely unexplored 30–300GeV band [4]. The large increase in sensitivity raises the distinct possibility to discover new phenomena and new types of gamma-ray sources. The LAT is being developed and built for a launch scheduled in

2007 by a multi-national collaboration, including scientists and engineers from France, Italy, Japan, Sweden, and the United States.

The LAT is a pair-conversion telescope, employing the same basic concept as EGRET. Utilizing silicon-strip detectors (SSDs) in place of the spark chambers of EGRET, it achieves great improvements of the sensitivity (6×10^{-9} ph $cm^{-2}s^{-1}$) by means of increased effective area (8,000 cm^2), a much larger field-of-view (2 sr), and improved angular resolution (3.5 degree at 100 MeV, 0.15 degree at 10 GeV). The SSD tracker has great advantages compared with spark chambers including: (1) self-triggering, which simplifies the system and enables the LAT to achieve a maximum field-of-view limited only by the tracker geometry, (2) fine-pitch strip spacing, which provides excellent track-recognition information for background rejection and reconstruction of the conversion pair, (3) high-density optimal packing of detectors to minimize the negative impact of multiple scattering, (4) close to 100% efficiency of detection of relativistic particles, due to the high signal-to-noise ratio, (5) fast response and readout, enabling almost dead-time free operation, and (6) no consumable gases.

The main design issues of the LAT derive from the requirements of a space application, where payload mass and available electric power are strictly limited and extremely high reliability is required. To simplify the production and maintain redundancy, a highly modularized structure is implemented in the LAT design. The LAT is composed of a 4×4 array of tower modules, each composed of a silicon tracker (TKR) and a CsI calorimeter (CAL). The Anti-Coincidence Detector (ACD) surrounds the entire set of tower modules. The layout is illustrated in Figure 1. An exploded view of a single TKR tower is shown in Figure 2. Assembly of the trays and TKR towers is being done in Italy by INFN institutes working with commercial vendors [6]. See [6] for details of the TKR geometry and mechanical structure.

2 Front-end readout electronics module

The readout electronics for an SSD plane are contained on a single printed wiring board, forming a 'Multi-Chip Module (MCM)'. The MCM is implemented in standard chip-on-board technology. The one special feature in it is the Kapton pitch-adaptor flexible circuit. To minimize the gap of sensitive area between LAT tower modules, the MCM board is mounted vertically on the tray at the edge of the SSD plane. The pitch-adaptor flexible circuit is bent by 90° at the corner along a machined radius and connects amplifier inputs on the MCM to strips on a SSD plane via metal traces and wire-bonds. To satisfy requirements for power consumption and noise level, the MCM utilizes two custom ASICs: the GTFE (Glast Tracker Front-End chip) and the GTRC

(Glast Tracker Readout-Controller chip). These GTFE and GTRC ASICs were developed exclusively for this mission [7]. Both of the ASICs are implemented in the Agilent 0.5-μm CMOS process. An MCM carries 24 GTFE chips and two GTRC chips. Figure 3 shows a schematic diagram of the TKR control-and-readout electronics and Figure 4 shows a picture of an MCM board.

One GTFE chip contains 64 channels of charge-sensitive amplifiers, each followed by a comparator. A common threshold of the comparators per chip can be controlled with a 7-bit DAC. The chip also has an internal calibration system, which includes a 7-bit DAC to set the level of the injected charge and a 64-bit register to select any subset of channels to inject charge into. Two 64-bit mask registers are located on the channel outputs, to allow any subset of channels to be disabled from the trigger output or from the data stream. The trigger output is simply a logical-OR of all 64 channels. The event data stream includes only those channels with amplified signals exceeding the threshold. The data is stored into a 4-deep event buffer and read-out by a simple shift register, with an additional zero-suppression feature. To handle 1536 signals on a single SSD layer, 24 GTFE chips are held on an MCM.

GTRC chips act as an interface between the GTFE chips and the base data acquisition electronics module, TEM (Tower Electronics Module), placed at the bottom of the CAL. Command, trigger, and clock signals from the TEM are buffered by the GTRC before going to the GTFE chips. The GTRC chip formats, zero suppresses, and buffers the data from the GTFE chips before sending it to the TEM. It also measures the time-over-threshold of the trigger signal, which can be useful for background rejection (to distinguish charge deposition of two electrons from that of a single relativistic particle and to reject stopping nuclei). An MCM board carries two GTRC chips, providing two redundant control/readout paths to the GTFE chips.

We built a prototype TKR tower composed of only 5 trays, using ASICs from the flight production, and tested it to verify the performance. The test results showed that the power consumption is 160 μW per channel, including the digital readout circuits, and the noise equivalent charge is less than 2000 electrons RMS under the capacitive load of 36-cm long strips at the amplifier input, which confirmed that the system meets the requirements. Table 1 summarized the design parameters and verified performance of the TKR front-end electronics MCM.

3 Tests of front-end and readout-controller ASICs

All flight ASICs were tested on the wafers with a wafer-probe station at UCSC/SCIPP before dicing, and defective chips were screened. Power con-

sumptions and all digital functionality including functions of all control registers, data buffers and output line drivers, were tested. As for GTFE chips, liveness and gain of all 64 amplifiers were also tested. In the test of the GTFE, 122 wafers, each including 181 chips, were tested, and the yield was 95.2 %. As for GTRC, 19 wafers, each including 297 chips, were tested, and the yield was 87.6 %.

We also tested radiation hardness of these ASICs by heavy-ion beams and ^{60}Co in INFN-Legnaro, Italy facility [9]. Regarding single-event latch-up (SEL), we verified that the SEL threshold is well above a Linear Energy Transfer (LET) of 60 MeV cm^2 mg^{-1}. Single-event-upset (SEU) is an issue for the configuration registers in this system, so we employ a radiation-hardened design for these [8]. We verified that the SEU threshold is above the NASA required minimum of 8 MeV cm^2 mg^{-1}. Total dose measurements of up to 40 krad confirmed that the readout ASICs are sufficiently radiation hard for the GLAST mission.

4 Production and Tests of Multi-Chip Modules

Production of MCMs are being done at Teledyne Microelectronic Technologies Inc, Stanford Linear Accelerator Center (SLAC) and UCSC/SCIPP. Visual inspection and tests of electrical functionality including load/readback of control registers on all GTRC and GTFE chips, transmission of the data and the trigger signals in the unit, and liveness of the entire 1536 amplifiers, are performed at each critical step during production, before and after encapsulation of the ASICs. The precise measurement of gain and noise of all channels is performed for the first time in this step, and dead/noisy channels are detected. MCMs passing all screening criteria are shipped to SLAC. Burn-in tests at 85°C, temperature cycle tests, and functionality tests at three temperatures, −20°C, 25°C and 60°C, are done there. Then, finally, all the functionality tests and measurements of gain and noise are repeated, and units passing all the tests are shipped to Italy for integration into the flight towers.

Before starting production of flight MCMs, we completed 50 preproduction MCMs to validate the manufacturing process. As of July 15, 2004, 172 MCM units for flight production were completed. Figure 5 show the distribution of the gain and noise of all channels of the 172 MCM units. Note that these are the values measured under no capacitive load on the amplifier inputs. The gain variation is 12 % RMS. From the data analysis, we found that the variation is mainly from chip-to-chip while the variation within each chip is less than 6 %. Note here that this measured variation of the measured gain include contributions from the variation of the calibration components, such as test capacitors on the amplifier inputs to inject test charge. The bad (dead/hot/noisy) channel rate of these MCM units is 1.55×10^{-4}, which is

comparable to the bad strip rate in the SSD [10] and is sufficiently low to meet the LAT requirements.

5 Conclusions and Status

The GLAST mission, with at least a 30-fold improvement in sensitivity over the previous high-energy gamma-ray mission, promises large gains in our knowledge and understanding of high-energy astrophysics, particularly non-thermal process occurring around some of the most exotic objects in the universe. This large improvement is achieved by application of modern silicon-strip detector technology. To satisfy requirements for power consumption, noise level and radiation hardness in the space environment, two kinds of custom ASICs are utilized in a tracker front-end electronics module. Tests with pre-production test units and a prototype tracker tower confirmed that the system meets the requirements. For the launch in 2007, production and tests activities for flight tracker towers are now ongoing, such as (1) MCM Production at Teledyne, (2) Burn-in and temperature cycle tests of MCMs at SLAC, (3) Kapton flex-circuit cable production at UCSC and SLAC, (4) Tray assembly and test in Italy, (5) Composite tray panel and sidewall fabrication in Italy, and (6) Tower assembly and test in Italy. The first tracker tower module will appear in September, 2004.

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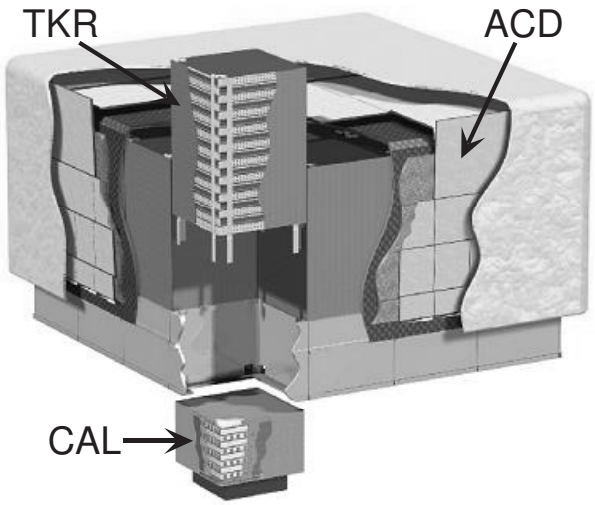

Fig. 1. Design of the GLAST LAT instrument.

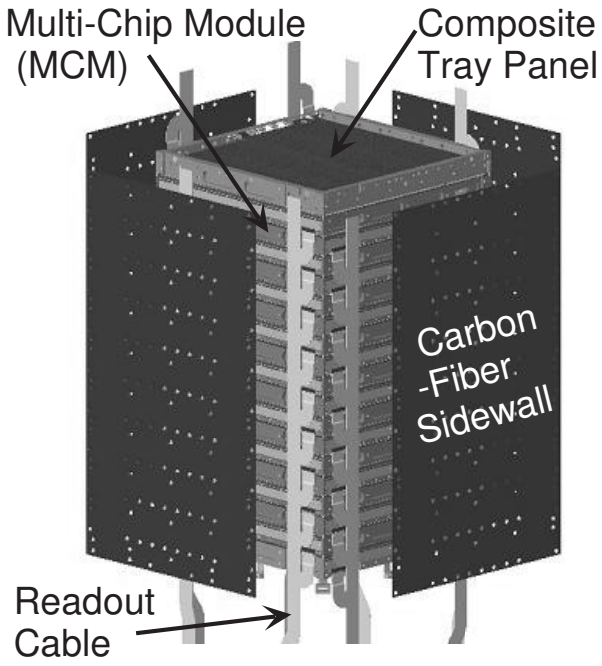

Fig. 2. Exploded view of a single TKR tower.

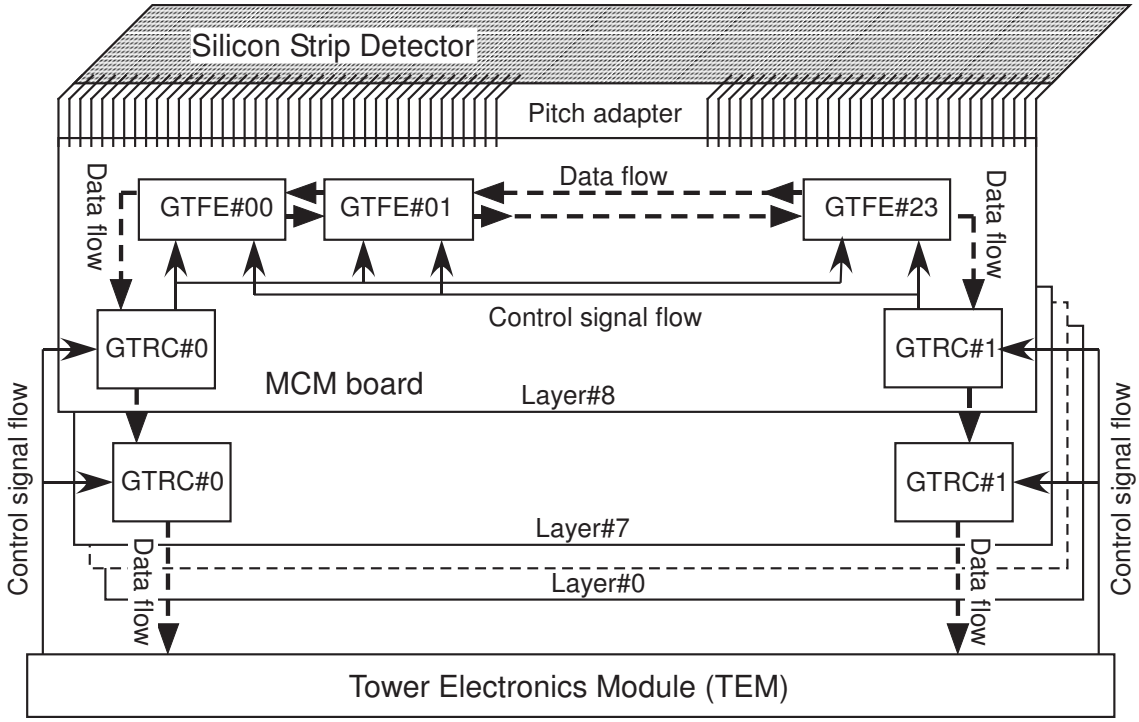

Fig. 3. Schematic diagram of the TKR control-and-readout electronics

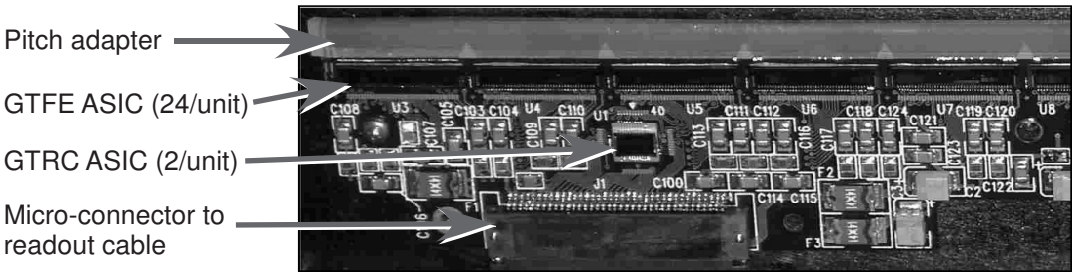

Fig. 4. MCM before encapsulation of ASICs.

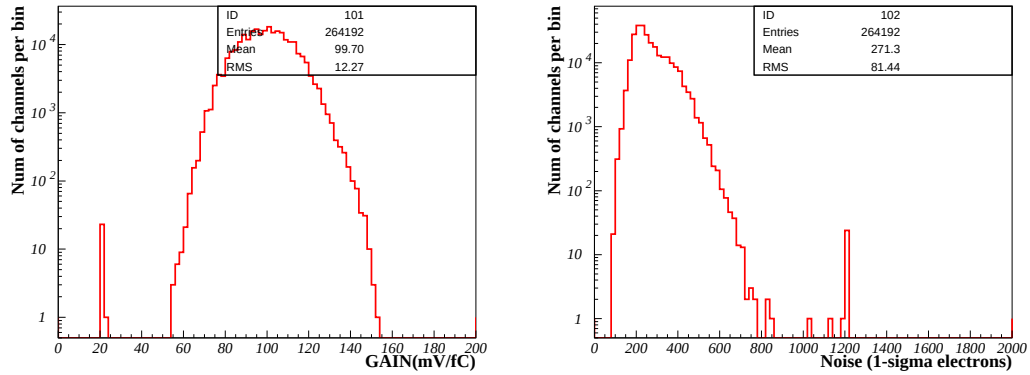

Fig. 5. Gain (left panel) and noise (right panel) distributions of all channels of the MCMs built by 15 July 2004, measured under no capacitive load on the inputs.

Table 1
Design and performance of TKR front-end electronics MCM

Parameter	
ASICs on board	2 GTRC + 24 GTFE
Power voltage	2.5 V (digital), 1.5 V, 2.5 V (analog)
Output signal	Data flow of hit pattern of 1536 channels and TOT (Time Over Threshold) per layer, Fast logical OR of entire channels for trigger
Number of channels	1536 (64/GTFE $\times$ 24)
Power consumption	130 mW (digital), 120 mW (analog)
Noise equivalent charge at 30 pF capacitive load (typical)	1500 electrons (RMS)