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GLAST LAT Tracker ASIC Review

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I. Findings

1. Front-End Analog ICs

Both the GTFE-G and GTFE-F2 are functional, but both show behavior that precludes a decision on the flight IC at this time. Several characteristics of these ICs merit further investigation, but at this point I concentrate on the major roadblocks to flight acceptance.

1.1. GTFE-F2

The threshold scan curves show a “ragged” behavior, which indicates some form of cross-talk. This phenomenon appears to be related to occupancy, as calibration scans triggering 8 channels simultaneously show better results than scans with 32 channels. The threshold dispersion also increases when more channels are scanned simultaneously. The last two channels of each IC are especially afflicted. In the experiment occupancies will be lower than in the threshold scans performed to date, so these results are not necessarily fatal for the experiment.

The noise levels derived from the threshold scans (~ 2000 e) are higher than simulated and also higher than measured on the GTFE-G (~1500 e). However, the data shown for noise rate vs. threshold show approximately the same noise performance for both ICs, so the higher noise may be an artifact of the threshold problem. Depending on the cross-talk mechanism, modifications to the MCM could improve performance, but that is not clear at this time.

The layout of the GTFE-F2 shows several areas where cross-talk could dynamically affect the comparator thresholds. A revised layout has been completed.

1.2. GTFE-G

The GTFE-G shows acceptable performance, except that roughly 20% of the ICs oscillate at unacceptably high threshold settings. Disabling the “threshold conditioner” appears to solve this problem, although the
reason is not yet understood.

2. Digital Readout IC

The GTRC could not be tested at the wafer level, so yields are not available. However, they appear to be acceptable, but this must be verified. GTRC ICs have been tested in “quite a few” mini-MCMs and in three full-sized MCMs. The major problem is the lack

of timing margin. Margin can be recovered by increasing the supply voltage (and overall power dissipation) or reducing the clock frequency. The IC appears to function as designed, but since not all eventualities can be simulated, further system tests are needed to verify sufficient robustness for flight. The functions have been replicated in an FPGA to further analyze the problem. Proposed circuit changes have been implemented in the FPGA and verified.

3. Ladders and Trays

Front-end ICs were tested using mini-MCMs connected to a full-length ladder. Two ladders are of high quality, whereas the third suffered from a relatively large number of defective detector strips, which is attributed to faulty coupling capacitors incurred during wire-bonding. In addition, ICs have been provided to Pisa for the fabrication of three complete trays with both sides populated and 2 trays with one side. These engineering models are expected in mid-January. This will allow extensive tests on a representative part of the full system.

II. Recommendations

The following recommendations seek to maintain the schedule while ensuring the quality required for launch. The rationale is to submit new wafer runs that could provide ICs for production. By submitting both GTFE-F2 without changes and GTFE-G with a “minor” change (GTFE-G2), one could obtain one design with acceptable performance. Since both ICs require further tests, the test program should continue unabated and expand to include the tray engineering models due in January. A decision on which IC to use for the flight hardware depends on many considerations, but it may have to await completion of the proposed fabrication run and complete testing of both ICs. The GTRC could be usable at a reduced clock rate or higher supply voltage, but this must be investigated further. Revised designs should be submitted in parallel with the analog ICs.

Specific recommendations (unless a chip version is specified, recommended measurements apply to all versions). GTRC related recommendations are grouped at the end.

1. Develop a plan to determine quantities of ICs required vs. time.

   This will determine to what extent revised ICs could be incorporated. For example, some trays could be populated with “first generation” production ICs and others with improved ICs to increase robustness.

2. Submit wafer fabrication runs for GTFE-F2 (without changes) and GTFE-G2 (GTFE-G without the “threshold conditioner”).

Rationale: The GTFE-F2 may be usable as is, if good threshold performance can be demonstrated at low occupancies, so this provides a “no change” option. GTFE-G would be acceptable, except for uncertainties in the behavior of the “threshold conditioner”. Since no compelling case was made for the inclusion of this circuit element, it should be removed. As this is only an ancillary circuit element, the key functionality of the IC could be unaffected. However, this “minor modification” is a change and carries some risk.

3. Continue the measurement program at full scope and expand it to include the tray engineering models being assembled in Italy.

4. Investigate GTFE-F2 behavior at low occupancy

   Perform threshold/calibration scans on only one channel at a time. Investigate deterioration as number of scanned channels increases.

5. Measure noise occupancy vs. threshold and determine at which threshold level the occupancy deviates from gaussian noise. This indicates at which threshold level spurious pickup becomes important. This measurement should be performed on individual modules and – as a final check – at the tray level.

   See www-physics.LBL.gov/~spieler for a more detailed discussion, for example in the ICFA lectures in Morelia (“Rate of Noise Pulses in a Threshold Discriminator System” in the Appendices; see p. 42 for an example)

6. Take threshold scans over full dynamic range to derive full calibration curve and check if the measured noise corrected for the gain is constant. At low thresholds determine at which level the noise deviates from the expected response to assess level of spurious signals (e.g. cross-talk).

7. Determine the acceptable noise rate per IC to determine margin for noise level and threshold variations.

8. In the GTFE-G, disable the “threshold conditioner” on some good ICs to see if there is any effect. Repair some more defective ICs and measure their performance.

9. Submit for fabrication the revised GTRC (GTRC5). As a fall-back the existing GTRC could be included in the same reticle, possibly together with alternative new designs, depending on the perceived risk.

10. From systems considerations determine the minimum acceptable clock rate for the GTRC and compare with the maximum rate that provides sufficient timing margin.

11. Test the GTRC and readout system at high random trigger rates.

14. Verify functionality of GTRC wafer test system prior to arrival of new ICs.