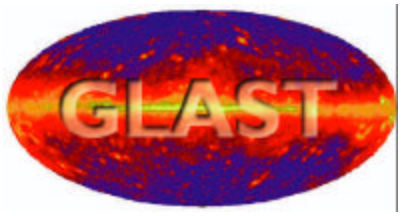	Document # LAT-TD-00249-10	Date Effective January 31, 2004
	Author(s) R.P. Johnson M. Sugizaki	Supersedes
GLAST LAT TECHNICAL DOCUMENT	Subsystem/Office Tracker	
Document Title **Tracker TMCM Test Plan and Procedure**		

Gamma-ray Large Area Space Telescope

(GLAST)

Large Area Telescope (LAT)

Tracker Subsystem

Tracker TMCM Test Plan and Procedure

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
1	August 21, 2001	Initial draft.
2	Nov. 2, 01	Added section on testing after mounting onto trays
3	Jan 3, 03	Add test of trigger passing in the TMCM
4	Jan 20, 03	Update qual testing and burn-in sections.
5	June 10, 2003	Update according to the actual test program
6	July 31, 2003	Remove everything except for MCM functional tests
7	August 21, 2003	Add descriptions of command sequence in functionality test Change the order of test items according to the practical operation
8	October 31, 2003	Update Figure 1.
9	November 6, 2003	Change allowed bad channels from 5 to 4. Edited the language a bit.
10	January 24, 2004	Change allowed bad channels to 8. Adjust cuts on the bad channel definition based on preproduction results.

Table of Contents

1. OBJECTIVE

This report serves to document the production test plan of the GLAST LAT Tracker front-end electronics readout modules (TMCM). It also documents the detailed software procedures executed during the test. This plan covers the functional testing of MCMs during production of the MCMs at the assembly vendor, both before and after encapsulation of the ICs and wire bonds. The procedure to be followed by the personnel executing the tests described in this document is found in [22]. The same procedure is executed following MCM burn-in and just prior to shipment to Italy, as documented in the burn-in procedure [24].

2. SCOPE

The GLAST LAT Tracker will be instrumented with about 80 m^2 of silicon strip detectors (SSD) and nearly 900,000 channels of electronics. The SSDs are assembled onto the two sides of composite "tray" panels, of which 19 are stacked into each of the 18 towers. Each layer of SSDs is read out by an electronics module (TMCM), mounted on the edge of the tray panel. Extensive testing of the electronics is done during assembly at the component level (ASIC and TMCM) and at the tray level. The overall electronics test plan and the hardware systems for those tests are described in [11]. The procedures for wafer testing of the ASICs to be mounted on TMCMs are documented in [15] and [16]. This plan covers the electrical testing of the TMCMs after all components have been mounted and wire bonding within the TMCM is complete. The environmental and electrical test plans of the completed towers are specified in [14] and [17].

The requirements being met by these tests are documented in the Tracker readout electronics requirements [4] and the Tracker Level-III specifications [2].

3. ACRONYMS AND DEFINITIONS

ASIC	Application Specific Integrated Circuit
DAQ	Data Acquisition System
GLAST	Gamma-ray Large Area Space Telescope
LAT	Large Area Telescope
MCM	Multi Chip Module
NCR	Non-Conformance Report
PWB	Printed Wiring Board
SSD	Silicon Strip Detector
TEM	Tower Electronics Module
TKR	GLAST LAT Silicon Tracker
TOT	Time over Threshold
Tracker	Silicon Strip Tracker of the LAT
Sensor	Silicon Strip Detector (SSD)

4. REFERENCES

[1] LAT-TD-00156 LAT Tracker Preliminary Design Report.

[2] LAT-SS-00017 LAT TKR Subsystem Specification–Level III Specification.

[3] LAT-SS-00134 LAT TKR Subsystem Specification–Level IV Specification.

[4]	LAT-SS-00152	LAT TKR Subsystem Specification–Level IV Readout Electronics Requirements.
[5]	LAT-SS-00168	Conceptual Design of the LAT Tracker Electronics Readout System.
[6]	LAT-SS-00169	Tracker Front-End Readout ASIC Specification.
[7]	LAT-SS-00170	Conceptual Design of the GLAST Tracker Readout Controller Electronics ASIC (GTRC).
[8]	LAT-SS-00171	Specification of the LAT Tracker front-end readout Multi-Chip Module (TMCM).
[9]	LAT-SS-00173	Tracker Grounding and Shielding Plan.
[10]	LAT-SS-00175	GLAST Tracker Flex Cable Specification.
[11]	LAT-TD-00153	Test Plan for the GLAST Tracker Front-End Electronics.
[12]	LAT-SS-00176	Tracker Electrical Interface Specification.
[13]	LAT-TD-00154	LAT Tracker Tray Test Plan.
[14]	LAT-TD-00155	LAT Tracker Tower Test Plan.
[15]	LAT-TD-00247	LAT Tracker Front-end Readout Chip Wafer Test Procedure.
[16]	LAT-TD-00248	LAT Tracker Readout Controller Chip Wafer Test Procedure.
[17]	LAT-TD-00191	LAT Tracker Tower Electrical Test Plan
[18]	LAT-DS-00180	LAT Tracker Tray Assembly with Payload
[19]	LAT-TD-01037	EM Trays Thermal Test Plan
[20]	LAT-TD-01004	EM Trays Vibration Test Plan
[21]	LAT-TD-00778	LAT Environmental Test Specification
[22]	LAT-PS-01971	LAT Tracker MCM Test Procedure
[23]	LAT-TD-02366	LAT Tracker MCM Qualification Plan
[24]	LAT-TD-02367	LAT Tracker MCM Burn-In and Acceptance Environmental Test Plan

5. TRACKER TOWER DESCRIPTION

The conceptual design of the Tracker tower modules is described in the Preliminary Design Report [1]. The conceptual design of the readout electronics is described in [5], and detailed specifications for the components of the design are found in [6], [7], [8], [9], and [10]. The electrical interface of the Tracker readout to the TEM is described in [12].

6. TEST SYSTEM

All of the tests described herein require the following ground support equipment (see [11] and Figure 1). Certain tests require additional equipment, as specified in the relevant sections.

- Connector savers attached to both TMCM connectors (these should remain in place following completion of the tests).
- PC with a VME interface card and a GPIB interface card, plus printer and CD writer.

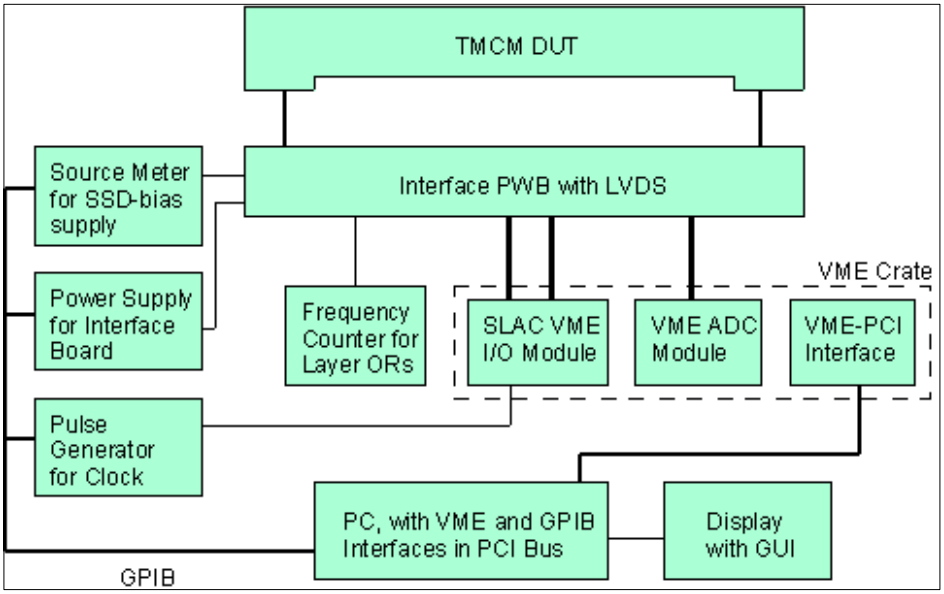

Figure 1. Block diagram of the system for TMCM testing.

- VME I/O module, VME crate, and crate controller.
- VME-based ADC module.
- Frequency counter in VME or with GPIB interface.
- Power supplies for the interface board (5 V) and SSD bias (100 V nominal, 150 V maximum). The supplies shall include adjustable voltage, current monitoring, adjustable current compliance, and a GPIB interface.
- Interface PWB with LVDS drivers and receivers. The data output lines and layer-OR lines are terminated with 100 Ω, and the token output lines are terminated with 1000 Ω. This board also includes the power supplies for the MCMs and analog buffers for measurement of LVDS DC levels.

7. ELECTRICAL ACCEPTANCE TESTING FOLLOWING TMCM ASSEMBLY

These acceptance tests are carried out on every TMCM at the assembly vendor after completion of the wire bonding and before application of encapsulation to the wire bonds. They are repeated following encapsulation and conformal coating.

7.1 TMCM POWER CONSUMPTION TESTS

7.1.1 Power Consumption

The TMCM is plugged into the test fixture. The digital power (2.5 V), analog high (2.5 V), and analog low (1.5 V) supplies are successively turned on. The resulting current draws are checked to be within specifications for both clock on and clock off and are recorded.

Test	Purpose	Specification (mA)	Prerequisite	Configuration
TM702	Measure the TMCM power consumption.	IDVDD = 50 ± 3 (add. 5) IDVDD = 51 ± 3 (add. 0) IAVDDA = 50 ± 3 IAVDDB = 13.5 ± 3	Visual inspection of completed TMCM.	TMCM mounted on assembly jig or handling fixture and covered.

1. Supply 2.5V on DVDD, 1.5 V on AVDDA, and 2.5 V on AVDDB.
2. Set the GTRC address to 0.
3. Explicitly set each GTFE calibration DAC and threshold DAC to the expected default power-on states (i.e. don't rely on the power-on to set them).
4. Measure the current draw into DVDD, AVDDA and AVDDB in a clock-off state.
5. Supply a 20-MHz clock signal and measure the current draw in a clock-on state.
6. Set the GTRC address to 5 and repeat the measurements of steps 3-4.

7.1.2 SSD Bias and Leakage Current

The bias supply is turned on and ramped up to 200 V with the potential applied to the TMCM. The leakage current is verified to be less than the maximum allowed.

Test	Purpose	Specification	Prerequisite	Configuration
TM703	Measure the TMCM bias leakage current.	Current less than 100 nA at 200 V potential.	Visual inspection of completed TMCM.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Supply 2.5V on DVDD, 1.5 V on AVDDA, and 2.5 V on AVDDB and 20-MHz clock signal.
2. Turn the SSD bias on and measure the current draw into the SSD bias, DVDD, AVDDA, and AVDDB.
3. Increase the bias voltage up to 200 V by 10-V step and repeat the current measurement of step 2.

7.1.3 GTRC LVDS quiescent output levels

With the TMCM powered and supplied with a clock and address 0 applied to the GTRC address lines, the voltage of both sides of each LVDS output (data, token, and layer-OR for left and right GTRC chips) is digitized. The difference and the mean value of each pair are recorded and verified to be as expected for a logic-0 signal.

The address is reset to 5 and the measurement is repeated on the data line.

Test	Purpose	Specification (V)	Prerequisite	Configuration
TM708	Measure the GTRC LVDS output levels.	Mean = 1.25 ± 0.25. Diff = 0.13 ± 0.06 for	Power test TM702.	TMCM mounted on assembly jig or

		data of address 0, layer-OR, and token. Diff = 0.06 ± 0.06 for data of address 1.		handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Supply 2.5V on DVDD, 1.5 V on AVDDA, and 2.5 V on AVDDB and 20-MHz clock signal.
2. Set the GTRC address to 0 and measure the voltages of LVDS outputs.
3. Set the GTRC address to 5 and measure the voltages of LVDS outputs.

7.2 TMCM FUNCTIONALITY TESTS

Functionality tests in this section are performed in three clock frequencies, 14, 20, and 22 MHz.

7.2.1 GTRC Configuration Register and Readback

The left GTRC chip is addressed and its configuration registers loaded with a bit pattern. Then the register is read back and checked for any deviation from the expected pattern. The test is repeated with the complement of the input bit pattern. The test then is repeated with a broadcast address for writing the register, followed by readback and comparison.

The test is repeated for the right GTRC chip.

Test	Purpose	Specification	Prerequisite	Configuration
TM704	Test loading and readback of the GTRC configuration register.	Data read back must be identical to those written. Correct data packet and parity, as specified in [7].	Power test, TM702.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Apply a test script, TC202, in the GTRC wafer test procedure [16] for both the left and the right GTRC chips, and check the read-back data.

7.2.2 Selected GTFE configuration register load and readback

All 5 configuration registers of each GTFE chip are loaded with a bit pattern (the mode register bit for left-right control set to "left") and read back via the left-hand GTRC, one by one, with the GTFE chips individually addressed. The returned data are checked for any deviation from the expected pattern. The test is repeated with the complement of the input bit pattern.

The entire test is repeated using the right GTRC chip.

Test	Purpose	Specification	Prerequisite	Configuration
TM705	Test loading and readback of the GTFE configuration registers.	Data read back must be identical to those written. Correct data packet and parity, as specified in [7].	Power test, TM702.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into

				the test fixture.

1. Apply a test command sequence of TF202 in the GTFE wafer test procedure [15] for all the 24 GTFE chips from both the left and the right sides, and check read-back data.

7.2.3 Broadcast GTFE configuration register load

The GTFE mask and DAC registers are loaded with a bit pattern using a GTFE broadcast address sent via the left-hand GTRC, such that all 24 GTFE chips are loaded simultaneously. The patterns are then read back, one GTFE at a time, to verify the contents. The test is repeated via the right-hand GTRC.

Test	Purpose	Specification	Prerequisite	Configuration
TM706	Test loading and readback of the GTFE configuration registers in broadcast mode.	Data read back must be identical to those written. Correct data packet and parity, as specified in [7].	Register load and readback test, TM705.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Apply the load-GTFE-register command sequence of the test TM705 with the broadcast address (=31) and read back the registers of each GTFE chip one by one.
2. Check read-back data.
3. Repeat the test from both the left and the right sides.

7.2.4 GTRC addressing

The left GTRC configuration register is loaded with a bit pattern. The register is then read back using every address in the GTRC address space, each time setting the external GTRC address bits appropriately. For each address the data read back are verified to be the expected bit pattern. The test is repeated for the right GTRC.

Test	Purpose	Specification	Prerequisite	Configuration
TM707	Test that all address bits work for the GTRC chips.	In each case, the data read back must be identical to those written.	GTRC register load and readback test, TM704.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Set the external GTRC address on the cable signal to 5 and load a GTRC register with a non-default bit pattern (TOT_EN=1, FORCE_NO_ERR=0, READ_DELAY=5, OR_STRETCH=10, GTFE_CNT=21, SIZE=42, LD_FT=1, LD_DELAY=1, LD_STRETCH=1, LD_CNT=1, LD_SIZE=1).
2. Change the external GTRC address to 0 and send a read-GTRC-register command with a different GTRC address from 0 to 8.

3. Confirm that a response appears only in the case that the GTRC address is 0, which agrees with the external GTRC address.
4. Repeat the sequence 1 to 3 changing the external address from 1 to 8.

7.2.5 Hard and soft reset

Broadcast mode is used to load the GTFE and GTRC configuration registers with non-default bit patterns. The hard reset is pulsed, and then all of the configuration registers are read back, one by one. The software checks that the register information received corresponds to the power-on default. The test is repeated using the soft reset commands for the GTRC chips.

Test	Purpose	Specification	Prerequisite	Configuration
TM709	Test the hard and soft reset functions of the GTRC and GTFE chips.	The register information read back should match the default specifications in [6] and [7].	Register load and readback tests, TM704 and TM706.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Load the left-side GTRC register with a non-default bit pattern used in TM707.
2. Set all the GTFE chips to the right-hand mode with a broadcast address.
3. Send a reset pulse from the left side.
4. Read GTRC registers and confirm that the register configuration is returned to the default.
5. Read GTFE MUTE registers from the left side and confirm that it is returned to the left-hand mode.
6. Load a GTRC register with a non-default bit pattern again and send a reset command.
7. Read GTRC registers and confirm that the register configuration is returned to the default.
8. Repeat the steps 1-7 with a reset pulse and a reset command from the right side

7.2.6 Data propagation from the top to the bottom layer

Simulated data are sent to the GTRC data input and data outputs are read out. Check that the output data is agreed with the input data.

Test	Purpose	Specification	Prerequisite	Configuration
TM716	Test that data output coming from the above layer is propagated to the below layer.	The data coming from the above layer must be sent to the below layer without any errors.	GTRC register load and readback test, TM704.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Send a trigger-acknowledge with an event tag 0, and a token with a buffer number 0, each at proper timing.

2. In the same time, send simulated data, which is a bit stream of ones and zeros alternating each other, to the data input that receives data from the layer above.
3. Check that the token signal from the layer above appears following the blank strip data and that the simulated data start to appear in the data stream.

7.2.7 Trigger Propagation Test

All chips are set to send trigger and data to the left. One channel is enabled in one GTFE chip in the calibration mask and the calibration amplitude is set well above threshold. A calibration strobe is initiated and the program looks for a layer-OR signal from the left side. The time delay of the signal is also recorded. The process is repeated for each chip. Then all chips are set to go to the right and the entire process is repeated.

Test	Purpose	Specification	Prerequisite	Configuration
TM713	Test that the trigger output propagates successfully from each chip to the next. Also check the propagation delay.	All GTFE chips must be able to send their trigger signals to either the left or right GTRC.	Charge injection test, TM711.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Set all the GTFE chips to the left mode and disable all the GTFE mask registers using a broadcast address.
2. Enable for channel 8 the data, trigger, and calibration mask registers of an address-0 GTFE chip and set the calibration DAC to 42 in the low range and the threshold DAC to 32 in the low range. Also, set the address-0 GTFE to the deaf mode.
3. Send a calibration strobe command, a trigger-acknowledge with an event tag 0, and a token with a buffer number 0, each at proper timing.
4. Check that the layer-OR signal has one trigger request with a duration corresponding to OR-STRECH at proper timing.
5. Repeat steps 2 to 4 for all the 24 GTFE chips.
6. Repeat steps 1 to 5 in the right mode.

7.2.8 Readout Sequence with Charge-Injection

The GTFE chips are configured to read out to the left. The calibration mask is set to stimulate a set of non-adjacent channels just smaller in number than the GTRC buffer size, and the test is repeated with enough new calibration masks to cover all channels. The data and trigger masks are set to enable the same set of channels. The threshold DACs all are set at equal values around 1.5 fC. The charge-injection DAC is set to about 3 fC. Four calibration-trigger-readout sequences are executed for each calibration mask, each sequence using a different GTFE event buffer, and channels that do not respond are noted. The presence of the Layer-OR signal is also checked. The data stream is checked for proper formatting and for the expected time-over-threshold (see Figure 4).

The test is repeated with all GTFE chips configured to read out to the right.

Test	Purpose	Specification	Prerequisite	Configuration

TM711	Test the calibration and readout systems and look for dead channels.	All channels should respond to the charge injection. All 4 event buffers should be functional. At least 16 chips from the left and 16 chips from the right shall have TOT within the acceptance range.	Threshold scan, TM710.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Set all the GTFE chips to the left mode and disable all the GTFE mask registers using a broadcast address.
2. Enable channels (0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60) of data, trigger, and calibration mask registers of an address-0 GTFE chip and set the calibration DAC to 42 in the low range and the threshold DAC to 32 in the low range. Also, set the address-0 GTFE to the deaf mode.
3. Send a calibration strobe command, trigger-acknowledge with an event tag 0, and token with a buffer number 0 in a sequence at proper timing.
4. Check that the read-back data has hit strips corresponding to the enabled channel and a time-over-threshold agreed with that expected.
5. Repeat steps 2 to 4 changing the channels enabled with (1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61), (2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62), and (3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63) and the event tag with 1, 2, and 3, respectively.
6. Repeat steps 2 to 5 for all 24 GTFE chips.
7. Repeat steps 1 to 6 in the right-hand mode.
8. Acceptable TOT ranges:
    a. 14 MHz: between 40 and 250 clock cycles
    b. 20 MHz: between 50 and 300 clock cycles
    c. 22 MHz: between 50 and 300 clock cycles

7.2.9 Channel and Trigger Mask Test

All channels are enabled in the calibration mask, and the calibration amplitude is set to its maximum value. All channels are disabled in the data and trigger masks, and all thresholds are set to about 0.5 fC. A calibration strobe is initiated, followed by a trigger, and the layer-OR and data are read out. The output data are checked to contain no hits and the layer-OR is verified to be quiet.

Test	Purpose	Specification	Prerequisite	Configuration
TM712	Test that all channels can be masked from the data and trigger.	It should be possible to disable any subset of channels from the data stream and/or layer-OR.	Charge injection test, TM711.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

1. Set GTFE chips with addresses 0 to 11 to the left-hand mode and chips with addresses 12 to 23 to the right-hand mode.
2. Disable all the channels of the data and the trigger mask registers in all the GTFE chips.
3. Enable channels (0, 13, 26, 39, 52) of the calibration mask in all the GTFE chips.
4. Send a calibration strobe command, trigger-acknowledge with an event tag 0 and token with a buffer number 0, each at proper timing.
5. Check that the read-back data has no hit strip and the layer-OR signal has no trigger request.
6. Repeat steps 3 to 5 shifting the channels enabled until all the channels are covered.

7.3 TMCM QUALITY TESTS

Quality tests are applied only to the MCMs that passed the functionality tests.

7.3.1 Threshold Scan of Layer-OR Rate

The GTFE chips all are configured to read out to the left, and the left-hand layer-OR output is routed to a frequency counter. All 64 channels of the trigger mask are enabled in one of the 24 GTFE chips. Set the threshold DAC to 10, 12, 14, 16, and 18, in the low range and measure the trigger-request (layer-OR) frequency in each threshold DAC. Repeat the test for all 24 GTFE chips.

Test	Purpose	Specification	Prerequisite	Configuration
TM715	Measure the layer-OR rate of each GTFE chip to check the noise level.	For a DAC setting of 10-low there must be zero noise hits in 0.5 seconds.	Trigger propagation test, TM713	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

7.3.2 Readout Sequence with Threshold Scan

A threshold scan can be done as follows. The GTFE chips are configured to split the readout equally between left and right. The data mask is set to enable a number of adjacent channels just smaller than the GTRC buffer size, and the test is repeated with new masks until all channels are tested. The threshold DACs are set to the minimum value and 1000 triggers are rapidly sent, each trigger followed by readout. The occupancy is calculated for each channel, and the procedure is repeated

with the next higher threshold DAC value. The data stream is checked for proper formatting, and the data from each channel are analyzed to extract a rough noise threshold.

Note, however, that the procedure outlined above is too time consuming to be practical during production testing, so the system is set to measure the occupancy only at a DAC setting of 10-low (about 0.5 fC), and the data mask is opened to all channels. No fitting is done, but excessively noisy channels are noted.

Test	Purpose	Specification	Prerequisite	Configuration
TM710	Test the readout and look for hot channels.	For a threshold DAC setting of 10 the occupancy of a good channel shall not be greater than 1 hit in 1000 triggers.	Register load and readback tests, TM704 and TM706.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

7.3.3 Threshold scan with charge injection

The GTFE chips are configured to split the readout equally between left and right. The calibration mask is set to stimulate a set of non-adjacent channels just smaller in number than the GTRC buffer size, and the test is repeated with enough new calibration masks to cover all channels. The data and trigger masks are set the same as the calibration mask, except that hot channels found in test TM710 are disabled from the trigger mask. The charge injection amplitude is set to about 1.5 fC, and the threshold DAC is set to a minimum value. 50 charge injections are carried out, with a trigger and readout following each. The occupancy is calculated for each channel and for the two layer-ORs. The procedure is repeated for each step of the threshold DAC, and then the threshold curves are fit to extract a gain and noise value for each channel and for the layer-OR. Channels with unusual gain or noise are noted (see Figure 2 and Figure 3).

Test	Purpose	Specification	Prerequisite	Configuration
TM714	Measure the gain and noise of each channel.	With essentially zero load on the inputs, all channels should have a gain between 50 mV/fC to 150 mV/fC and noise less than 0.15 fC.	All TMCM functional tests.	TMCM mounted on assembly jig or handling fixture and covered. Both TMCM connector savers plugged into the test fixture.

7.4 TMCM ACCEPTANCE CRITERIA

TMCMs are rejected if there is any missing functionality in any of the chips, not counting problems with individual channels. All GTFE chips must read out left and right and send layer-OR signals both left and right. All 4 event buffers in all chips must function. There may be no bit errors present in the data stream. In particular, no parity errors are allowed. The TMCM must function with all possible addresses. The LVDS output levels of all data, token, and layer-OR signals must be within specifications. The time-over-threshold counters must both give results within the expected range for a given calibration input pulse.

To be specific an acceptable TMCM must pass all of the tests TM702, TM703, TM704, TM705, TM706, TM707, TM708, TM709, TM712, TM713, TM715, and TM716 according to the criteria stated in the Specification column for each test (see above).

Test TM710, TM711, and TM714 test individual channels. Variations in performance are expected among the individual channels of a TMCM. See the appendix for plots of the relevant quantities. A channel is considered "bad" if at least one of the following statements is true:

- No response is obtained from the channel in test TM711.
- The channel is "hot," having occupancy greater than 0.1% for a threshold of about 0.5 fC, according to test TM710.
- The gain is outside of the range 50 mV/fC to 150 mV/fC in test TM714 (Figure 2).
- The noise is greater than 0.15 fC (940 electrons) in test TM714 (Figure 3).

TMCMs with more than 8 bad channels fail the test.

8. FINAL TEST

Following encapsulation of wire bonds and conformal coating of the MCMs, the same test routine as described in Section 7 is repeated. It is also repeated following MCM burn-in, just prior to shipment to Italy. Again, a maximum of 8 bad channels is allowed, including those found prior to encapsulation. Only those MCMs that pass the tests, according to the same criteria described in Section 7.4, are accepted for delivery to the LAT. MCMs that fail require submission of an NCR.

9. APPENDIX: DISTRIBUTIONS FROM PREPRODUCTION MCMS

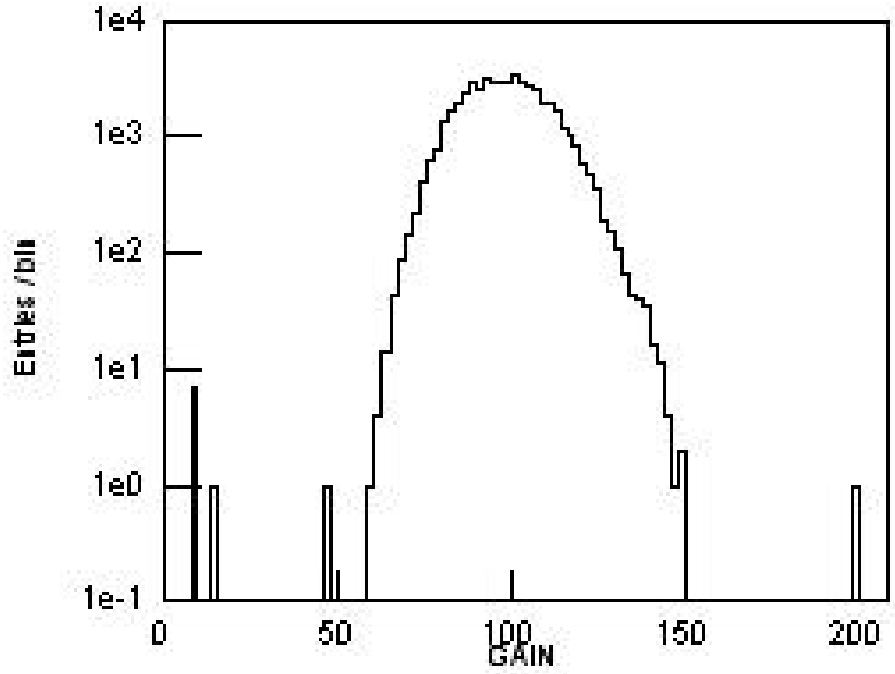

Figure 2. Distribution of channel amplifier gain, in mV/fC from about 30 preproduction MCMs (TM714).

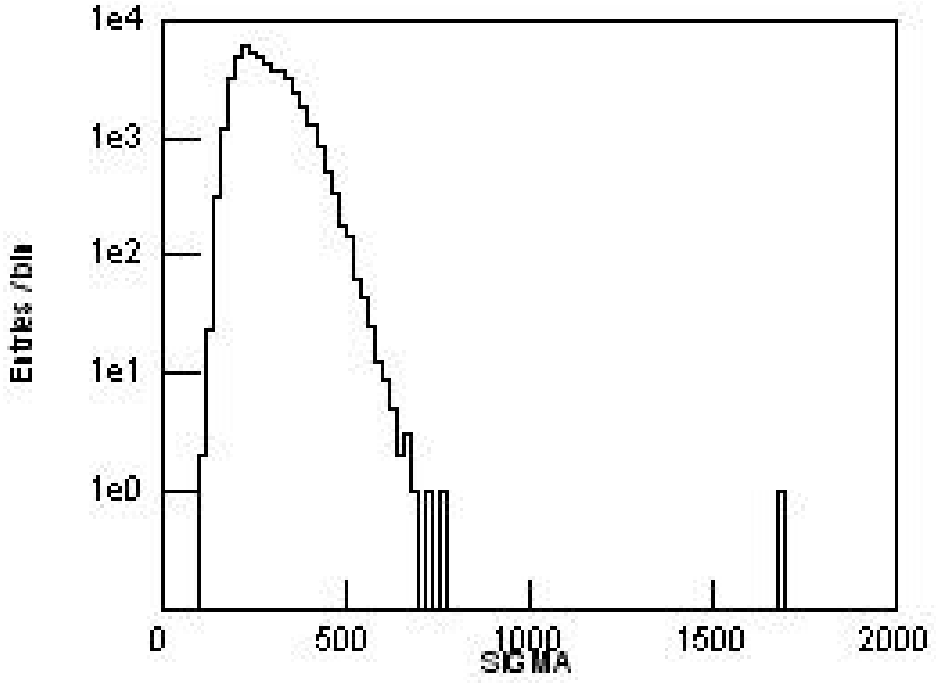

Figure 3. Distribution of channel amplifier rms equivalent noise charge (referenced to the amplifier input), in electrons, from about 30 preproduction MCMs (TM714).

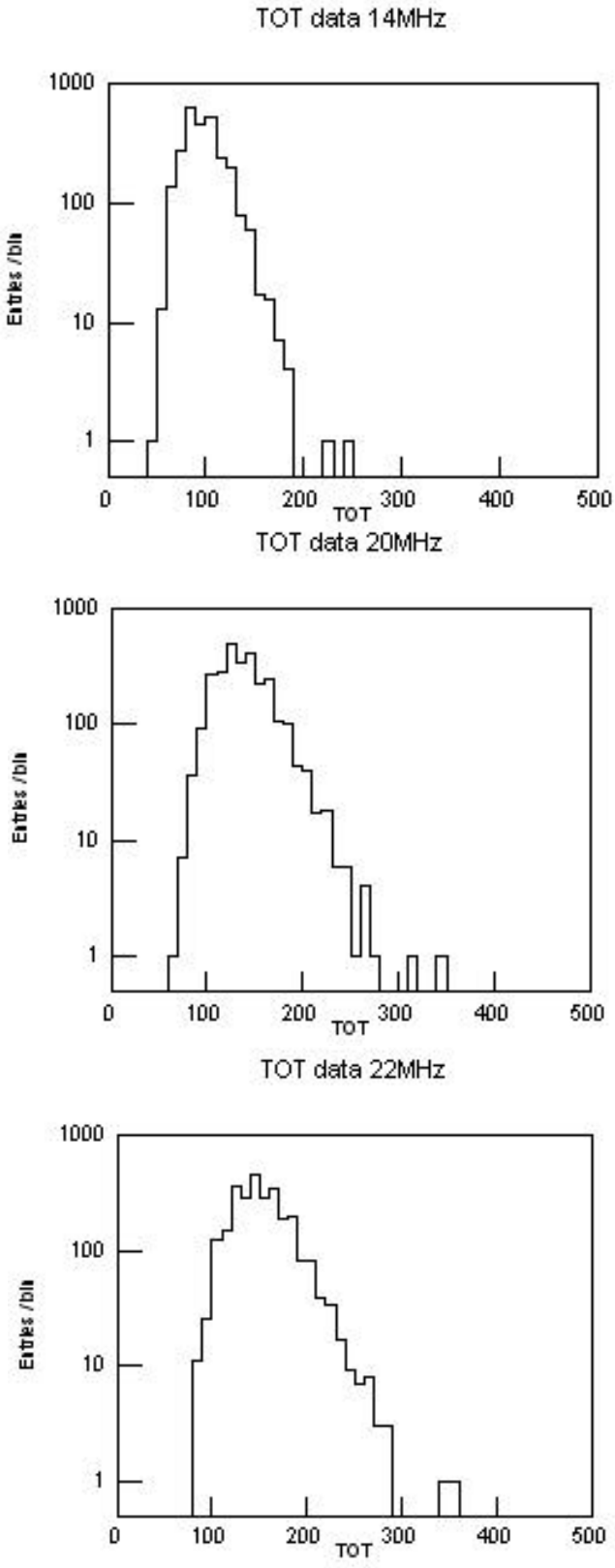

Figure 4. Time-Over-Threshold distributions, in clock cycles, from about 30 preproduction MCMs (Test TM711).