ACD_BFEM_Data_Format_V1.doc V1

Data Packet Internal Formats for the ACD Balloon Flight

This document describes the data to be recorded by the ACD on the balloon flight. This describes only packet internals which are found in the ACD 'directory' inside an ivtx packet, where x = e (event), h (housekeeping), or r (rate). The data is first described in block form and then details on the meanings of the fields are given below the blocks. The data is sequential - and the order is 1) right to left, then 2) down.
All numbers are unsigned integers.

There are three types of packets: 1) event data about level 1 trigger events, 2) housekeeping data regarding voltages and temperatures of ACD electronics and 3) rate counter data – rate of pulses above veto threshold seen from the scintillator tiles.

Event Data – 'acde'

Event data structure uses the full amount of FIFO information (17 32 bit words) stored in binary plus a global position time and position.

Description	*16 bit word*	*16 bit word*
Trigger counter	32 bit running counter	
Trigger timer	32 bit time in (50ns intervals?)	
Trigger Capture Word	lower 26 bits	
Veto Capture Word	lower 24 bits	
Pulse Height	Brd 0 Pmt 0	Brd 1 Pmt 0
Pulse Height	Brd 2 Pmt 0	Brd 3 Pmt 0
Pulse Height	Brd 4 Pmt 0	Brd 5 Pmt 0
Pulse Height	Brd 0 Pmt 1	Brd 1 Pmt 1
Pulse Height	Brd 2 Pmt 1	Brd 3 Pmt 1
Pulse Height	Brd 4 Pmt 1	Brd 5 Pmt 1
Pulse Height	Brd 0 Pmt 2	Brd 1 Pmt 2
Pulse Height	Brd 2 Pmt 2	Brd 3 Pmt 2
Pulse Height	Brd 4 Pmt 2	Brd 5 Pmt 2
Pulse Height	Brd 0 Pmt 3	Brd 1 Pmt 3
Pulse Height	Brd 2 Pmt 3	Brd 3 Pmt 3
Pulse Height	Brd 4 Pmt 3	Brd 5 Pmt 3
Dead Time Cause	lower 21 bits	

1) Trigger Counter Word (32 bits) running count of trigger event
2) Trigger Timer Word (32 bits) - clock ticks of FPGA for synchronization.
3) TREQ Capture Word - (32 bits & 0x03ffffff - lower 26 bits) all zeros except for trigger cause
4) bit 25: CPU TREQ - 1 if triggered by CPU

5) bit 24: EXT TREQ - 1 if trigger by external BNC input.
6) bits [23...20] - Board 5 PMTs [3...0]
7) bits [19...16] - Board 4 PMTs [3...0]
8) bits [15...12] - Board 3 PMTs [3...0]
9) bits [11...8] - Board 2 PMTs [3...0]
10) bits [7...4] - Board 1 PMTs [3...0]
11) bits [3...0] - Board 0 PMTs [3...0]
12) VETO Capture Word (32 bits & 0x00ffffff - lower 24 bits) - was event vetoed? (1 if PMT veto seen, else 0)
13) bits [23...20] - Board 5 PMTs [3...0]
14) bits [19...16] - Board 4 PMTs [3...0]
15) bits [15...12] - Board 3 PMTs [3...0]
16) bits [11...8] - Board 2 PMTs [3...0]
17) bits [7...4] - Board 1 PMTs [3...0]
18) bits [3...0] - Board 0 PMTs [3...0]
19) Then 24 unsigned 16 bit PHA values which must be compared with calibration runs to convert into energies.
20) Brd 0 ADC 0 (16 bits)
21) Brd 1 ADC 0 (16 bits)
22) Brd 2 ADC 0 (16 bits)
23) Brd 3 ADC 0 (16 bits)
24) Brd 4 ADC 0 (16 bits)
25) Brd 5 ADC 0 (16 bits)
26) Brd 0 ADC 1 (16 bits)
27) Brd 1 ADC 1 (16 bits)
28) Brd 2 ADC 1 (16 bits)
29) Brd 3 ADC 1 (16 bits)
30) Brd 4 ADC 1 (16 bits)
31) Brd 5 ADC 1 (16 bits)
32) Brd 0 ADC 2 (16 bits)
33) Brd 1 ADC 2 (16 bits)
34) Brd 2 ADC 2 (16 bits)
35) Brd 3 ADC 2 (16 bits)
36) Brd 4 ADC 2 (16 bits)
37) Brd 5 ADC 2 (16 bits)
38) Brd 0 ADC 3 (16 bits)
39) Brd 1 ADC 3 (16 bits)
40) Brd 2 ADC 3 (16 bits)
41) Brd 3 ADC 3 (16 bits)
42) Brd 4 ADC 3 (16 bits)
43) Brd 5 ADC 3 (16 bits)
44) Dead Time Cause (32 bits & 0x001fffff - lower 21 bits)
45) (bit 20) Readout L1T wait
46) (bit 19) CPU busy
47) (bit 18) FIFO Full Trap

48) (bit 17) FIFO Full
49) (bit 16) FIFO Half Full Trap
50) (bit 15) FIFO Half Full
51) (bit 14) ACD readout busy
52) (bits [13...0] Deadtime counter (x 50 ns)

Housekeeping Data – 'acdh'

Housekeeping data is all in 16 bit words, even though only 12 bits are used inside the ACD. There are 11 pieces of information (different voltages and temperatures) for each PMT channel, so for 24 channels we use 24 (pmts) x 11 x 16 = 132 x (32 bit words) for each housekeeping item. There is also one set of high voltage information for each cable (or board) that the TEM can handle. Each set of HV includes 4 measured voltages, so with 6 possible boards we have 6 (cables) x 4 x 16 bits = 12 x 32 bits more (total of 144 bytes). Using 2 more 32 bit words for time makes 144 + 2 = 146 32 bit words for each housekeeping read cycle. Housekeeping read cycles about every minute.

Order: Brds [0,1,2,3,4,5] for PMT 0, Brds [0,1,2,3,4,5] for PMT 1,
Brds [0,1,2,3,4,5] for PMT 2, Brds [0,1,2,3,4,5] for PMT 3

HSK DATA PACKET (580 bytes)
Sytem Time in clock ticks (32 bits) = 4 bytes
GPS (unix format) UTC Time stamp. (32 bits) = 4 bytes
ACD Electronics HSK data (24 x 11 x 2 [16 bits]) = 528 bytes.
ACD HV HSK Data 6 x 4 x 2 [16 bits] = 48 bytes

ACD Electronics HSK Data (each block is 16 bits)

Descr. / brd #pmt #	***O0***	***10***	***20***	***30***	***40***	***50***	***O1***	***11***	***21***	***31***	***41***	***51***	***O2***	***12***	***22***	***32***	***42***	***52***	***O3***	***13***	***23***	***33***	***43***	***53***
VREF																								
PHA_VREF																								
MIDAMP																								
PREAMP_OUT																								
PHA DISCR THRESH.																								
HIGH DISCR THRESH.																								
VETO DISCR THRESH.																								
TEMP_HOT																								
TEMP_BRD																								
PHA_FOLLOW																								
PHA_ADC_IN																								

ACD HV Hsk Data comes only from channel 0 of the board connected to Bertan HV power supply. Although we consider ourselves reasonably intelligent, we worry about the possibility of connecting the wrong cable to the board controlling the HV, so we will

command all boards to enable HV and will collect housekeeping from all boards. (We can also consider sending the data from channel zero of all boards to allow us the freedom to change which board will run the power supply without thought.)

Description	***size***
HV_ENABLE cable #0	16 bits
HV_IMON cable #0	16 bits
HV_CMD_DAQ cable #0	16 bits
HV_MON cable #0	16 bits
HV_ENABLE cable #1	16 bits
HV_IMON cable #1	16 bits
HV_CMD_DAQ cable #1	16 bits
HV_MON cable #1	16 bits
HV_ENABLE cable #2	16 bits
HV_IMON cable #2	16 bits
HV_CMD_DAQ cable #2	16 bits
HV_MON cable #2	16 bits
HV_ENABLE cable #	16 bits
HV_IMON cable #3	16 bits
HV_CMD_DAQ cable #3	16 bits
HV_MON cable #3	16 bits
HV_ENABLE cable #4	16 bits
HV_IMON cable #4	16 bits
HV_CMD_DAQ cable #4	16 bits
HV_MON cable #4	16 bits
HV_ENABLE cable #5	16 bits
HV_IMON cable #5	16 bits
HV_CMD_DAQ cable #5	16 bits
HV_MON cable #5	16 bits

Time stamps:

1) System clock ticks – the number of ticks of the system clock (runs at 100 Hz) since last reboot.
2) Last GPS time (within one second) at the time the HSK read started. The format is in unix 32 bit UTC time (seconds elapsed since Jan. 1, 1970 00:00:00).

Detailed description of ACD Electronics HSK items

1 VREF reference Voltage - The main reference voltage for all electronics. Should be about 2500 mV

2 PHA_VREF - the voltage at the PHA analyzer - should be ~2500 mV

3 PREAMOUT - Voltage level after the Preamplifier - should be ~2500 mV. Preamps on boards only being used by Gamma Target experiment - ACD uses preamps near PMTs.

4 PHA_DISCR_THR - The voltage setting the PHA discriminator for what level of

signals should be analyzed. This datum is roughly the value set by the phathr command + VREF.

5 HIGH_DISCR_THR - the voltage setting of the CNO discriminator. This datum is roughly the value set by hithr command + VREF.

6 VETO_DISCR_THRESH (called DISCR_THRESH in electronic schematics) - the voltage setting of the low (veto) threshold. This datum is roughly the value set by the lothr command + VREF.

7 TEMP_HOT - the temperature (K) of the Voltage Regulator

8 TEMP_BRD - the temperature (K) at the middle of the electronics for that channel. (Note this is confusingly called TEMP_VREF in the electronic schematics.)

9 PHA FOLLOW - voltage at the PHA follow-on electronics. should be about 2500 mV

10 PHA_ADC_IN - the offset voltage above vref at the input to the analog to digital converter - should be about 100 mV. This ensures that the even a PHA of 0 will give a positive signal

HV Hsk Item descriptions:

1. HV_ENABLE - the high voltage is off if value is ~5000 mV, and on if ~0 mV opposite to the way you would intuitively expect it. The enable command connects one of the control lines to ground - so the voltage goes to 0.

2.HV_IMON - the current being supplied by the HV power supply. The value goes from 0 - 5000mV (corresponding to 0 mA to max output of Bertan HV supply).

3. HV_CMD_DAQ - the value of the HV control voltage (this goes from 2.5V - 5V which corresponds to ~750V - 1500V out of the Bertan power supply). (Note this is called the HV_CMD_DAC in electronic schematics.)

4. HV_MON - for monitoring the HV output of the power supply (same units as HV_CMD_DAQ)

Rate Counter Data – 'acdr'

There is a 16 bit veto counter for each PMT. The time interval over which the counting is done is configurable - either 0.01 0.1 s, 1 s, or 10 s. If the rate counters overflow, then the counters will latch with all bits on, i.e. 0xffff = 65535 counts. During flight we will use only the time interval of 1 s so the rate would have to be > 65.535 kHz to overflow. The entire packet information is 14 * 4 = 56 bytes.

Description	***16 bits***	***16 bits***
System Time		
GPS UTC time		
Altitude x 10 (m)	(Signed 32 bit int)	
Time interval setting		
Rates 00 & 10	Cable 0 pmt 0	Cable 1 pmt 0
Rates 20 & 30	Cable 2 pmt 0	Cable 3 pmt 0
Rates 40 & 50	Cable 4 pmt 0	Cable 5 pmt 0
Rates 01 & 11	Cable 0 pmt 1	Cable 1 pmt 1
Rates 21 & 31	Cable 2 pmt 1	Cable 3 pmt 1
Rates 41 & 51	Cable 4 pmt 1	Cable 5 pmt 1
Rates 01 & 11	Cable 0 pmt 2	Cable 1 pmt 2
Rates 21 & 31	Cable 2 pmt 2	Cable 3 pmt 2
Rates 41 & 51	Cable 4 pmt 2	Cable 5 pmt 2
Rates 01 & 11	Cable 0 pmt 3	Cable 1 pmt 3
Rates 21 & 31	Cable 2 pmt 3	Cable 3 pmt 3
Rates 41 & 51	Cable 4 pmt 3	Cable 5 pmt 3

Rate Packet fields:

1) The system time. The number of clock ticks since last boot. The clock runs at 100 Hz.
2) The GPS UTC time. The time taken from the GPS during the previous second in unix UTC time format (seconds since Jan. 1, 1970 00:00:00).
3) Altitude in meters times 10. Height is defined above the GPS ellipsiod.
4) The time interval consists of the 2 least significant bits of the Time interval setting word – can be obtained by 'anding' with hex value 0x00000003. The setting numbers and the time intervals over which counts are accumulated are given in the next table. Rates are then found by dividing the raw number for each channel by the time interval.

Time interval setting & 0x00000003	Time integration interval (secs.)
0x0	0.01
0x1	0.1
0x2	1.0
0x3	10.0

5) Rates for brd [0...5] x PMTs [0..3]. in the same order as the PMT fields in the event

data.