Interface Control Document

Between The

BFEM Calorimeter (NRL) and the

TEM Board (Stanford)

Supporting the

GLAST Balloon Flight

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NOTE: At this time, this is not strictly an interface control document but more a repository of useful information on the implementation of the calorimeter readout and the calorimeter TEM for the 2001 Balloon Flight. This includes both hardware and software issues relative to the operation of the calorimeter.

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1. Introduction

This document describes the interface between the CAL VME TEM board and the Calorimeter for the GLAST Balloon Flight. See the document, "Interface Control Document Between The Version 2 TEM Board (Stanford) and the Calorimeter Control Board (NRL) Supporting the GLAST Tower Beam Test" dated 15 Nov 1999, for additional description of the interface and signaling between the calorimeter and the TEM. That document is hereafter referenced as CALBTEM ICD.

The DAQ TEM board interfaces to four calorimeter control boards, one for each side (see Figure 1). In routing commands to the calorimeter the TEM software must select the controller board address for the command. In regard to triggered event data, the TEM interface for the calorimeter accepts 20 serial streams (pipes) of ADC measurements (5 from each of 4 sides) and merges them into a single event FIFO. Each pipe contains 8 ADC measurements in a fixed pattern. Each ADC is represented by a 16-bit word. The TEM FIFO is loaded with pairs of ADCs, forming 32-bit words. Each trigger or digitization from the calorimeter creates 80 32-bit words in the FIFO containing ADC values. This list is preceded by a 32-bit trigger event number which identifies the trigger, a 32-bit trigger timer word, and a 32-bit (13 useful) TREQ/Veto status word. After the 80 ADC values, a 32-bit deadtime measurement (18 useful bits) is appended. Thus 84 words are loaded into the event FIFO per digitization. In nominal operating mode for the calorimeter during the beam test, there will actually be 4 digitizations per trigger. These four digitizations are for the four energy domains supported by the front end electronics. In this case, 336 words will be loaded into the FIFO for each trigger.

2. Communication Protocols

2.1. *Event Data from the Calorimeter Control Board to the TEM Board*

Upon the receipt of a Level 1 Trigger signal from the TEM, the calorimeter initiates a digitization of all ADC channels. There are 40 ADCs per Calorimeter Control Board. The Calorimeter Control Board sends to the TEM the digitized pulse heights from all the calorimeter log ends. Each control board sends data simultaneously over 5 serial data lines (pipes). In normal operating mode, there is one digitized pulse height value per log end. Each pipe serially transmits a 128 bit (8 x 16) data packet. All pipes transmit simultaneously.

For calibration mode, four pulse heights are readout per log end. This is implemented as essentially 4 separate transmissions of data that look like for separate L1T events complete with header. The four event messages however have the same event ID. The contents of the ADC will of course change as the energy range is sampled in the 4 digitizations and subsequent

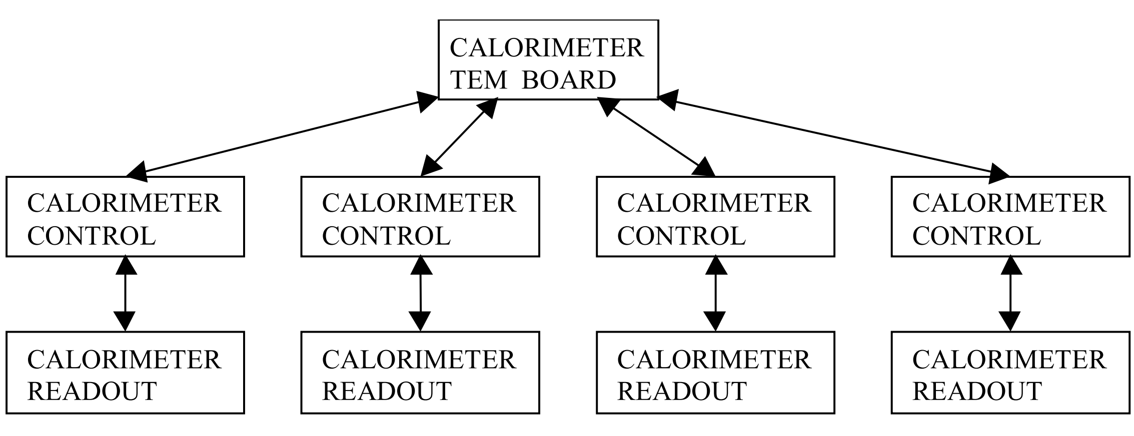

Figure 1 TEM-Calorimeter Communication Paths

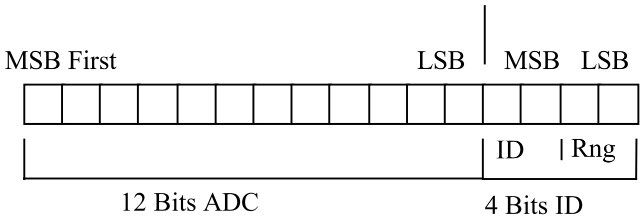

Figure 2. ADC data packet

transmissions.

Figure 2 indicates the organization of each 16-bit ADC values transmitted in the packet. The 12 bit ADC value is contained in the most significant bits. The remaining 4 bits encode the energy range of the channel (least significant 2 bits) and a sequence number (ID, adjacent 2 bits) for the ADC.

2.2. Commands from the TEM board to the Calorimeter Control Board

Commands are sent from the TEM to the Calorimeter for houskeeping functions and instrument mode settings. The TEM hardware adds the start bit and parity bit to a 16 bit value. Odd Parity bit is set by the hardware so that the base 2 summation of the command, data and parity bits is 1.

The TEM board has one command register for commanding the four calorimeter control boards. A multiplexor routes the serial data from the command register to the specified control board. The multiplexor is set by a control register (see CALBTEM ICD for register definitions) and must be set prior to writing the command in the TEM command register.

The 16-bit command word is shown in Figure 3. The most significant 8 bits identify a command function code. The least significant 8 bits contain a data value to be set for the specified command function. Not all command functions require a data value in which case the data field is ignored. The parity bit is added by the TEM hardware. The command functions are defined in Section 3.

2.3. Command Response from the Calorimeter Control Board to the TEM Board

Each command from the TEM board to the Cal Control Board results in a command response from the control board. The response consists of acknowledgements and optionally requested data. The length of the response message is variable, depending on command function. The acknowledgement is the repeated command function code and a status register as indicated in Figure 4. The command which requests the housekeeping readout of the rate counters results in a response of 41 16-bit words as shown in Figure 5, the acknowledgement and the 40 counter values..

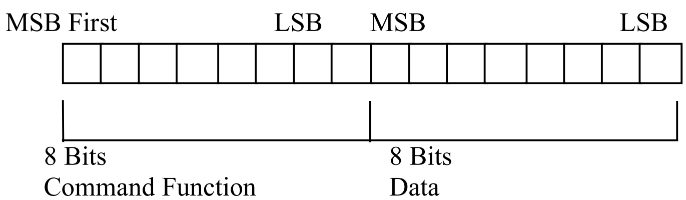

Figure 3. Command Word

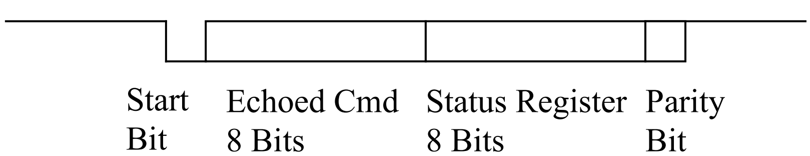

Figure 4. Command Return Format for Non Data Command

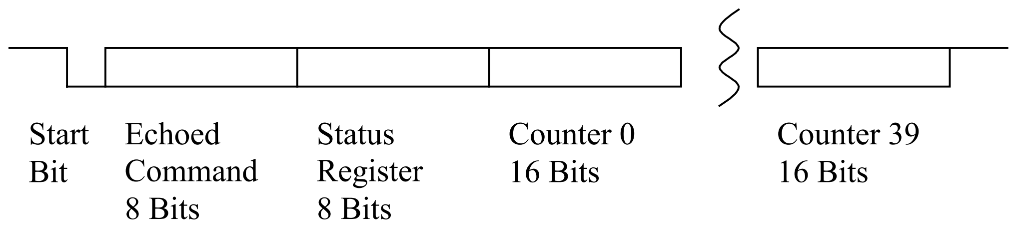

Figure 5. Command Return Format for Data Command Counter Readout

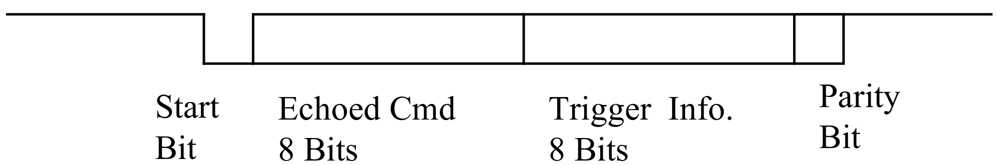

Figure 6. Command Return Format for Data Command Trigger Information

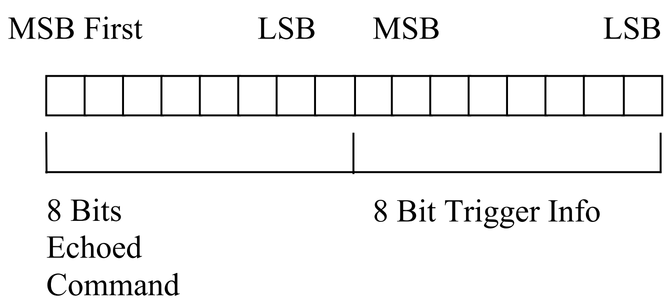

Figure 7 Command Return Word Format for Data Command Trigger Information

Table 1. Command Response Status Register Bits

Bit Position	Definition
0 LSB	Trigger Mode, See Table 4
1	
2	Data Readout Mode, See Table 5
3	
4	
5	Spare
6	Calorimeter Executed Command
7	Calorimeter Received Correct Parity

Table 2. Calorimeter Command Functions

Command Function, Hex	Command Description	Following Data Bits
00	Housekeeping Counters Readout	None
10	Load Input 0 Control Word	8 bit control word
11	Load Input 1 Control Word	8 bit control word
12	Load Input 2 Control Word	8 bit control word
13	Load Input 3 Control Word	8 bit control word
14	Load Input 4 Control Word	8 bit control word
20	Store DAC High Byte into Reg A	High Byte
21	Load DAC 0 Reg A + Low Byte	Low Byte
22	Load DAC 1 Reg A + Low Byte	Low Byte
23	Load DAC 2 Reg A + Low Byte	Low Byte
24	Load DAC 3 Reg A + Low Byte	Low Byte
30	Data Mode	3 bit data mode
40	Trigger Mode	2 bit trigger mode
~~50~~	~~Trigger Information 1, Rows~~	~~None~~
~~51~~	~~Trigger Information 2, Columns~~	~~None~~
60	Test Charge Injection	None
61	Pedestal Baseline Trigger	None
70	Extra Event Readout Dead Time	8 bit data – time tics
71	Rate Counter Dead Time	1 bit
F0 - FF	Reserved pseudo commands to CAL TEM	

3. Commanding of the Calorimeter Control Board

There are four control boards and associated front-end electronics boards (FEE). These four sides are labeled X-, X+, Y-, and Y+. See section 1 on the calorimeter coordinate system below. Table 2 summarizes the command functions recognized by the calorimeter control boards. The use of the command functions is discussed below. Commanding to the control boards utilizes the same TEM register for all four boards. A command can be sent to only one board per write to the command register. Consequently, a control register within the TEM must be set to select the appropriate control board for the command. Two bits in the control register set the command multiplexer to the desired cable. The physical wiring of the control boards to the TEM determine the relationship between multiplexer setting and addressed control board. The nominal definition of this relationship is CALMUX: 0 = X+, 1 = Y+, 2 = X-, 3 = Y-.

3.1. Housekeeping Counter Readout (0x00)

Each Cal control board contains 40 16-bit counters to monitor the threshold rate of each of the CsI log ends. The counters monitor the LowEn x4 lower level discriminator for each log; they are leading-edge triggered. The counters are active until receipt of the counter readout command. At that time, counting is disabled while the contents of all counters are transferred to output registers and the counters are cleared. Then counting resumes. The counter contents are transmitted to the TEM as described in section 2.3 (see Figure 5). The readout order of the 40 counters is summarized in section 8.

3.2. Crystal Control Word Programming (0x10 – 0x14)

Each of end of the 80 CsI crystals can be individually enabled for trigger processing. These enables are organized in 5 control words, one per readout pipe, for each calorimeter

Table 3. Relationship of enable bits in control words to crystal location.

Readout Pipe 0		Readout Pipe 1		Readout Pipe 2		Readout Pipe 3		Readout Pipe 4	
Control Word 0		Control Word 1		Control Word 2		Control Word 3		Control Word 4	
MSB Bit 7	Bit 3	MSB Bit 7	Bit 3	MSB Bit 7	Bit 3	MSB Bit 7	Bit 3	MSB Bit 7	Bit 3
Bit 6	Bit 2	Bit 6	Bit 2	Bit 6	Bit 2	Bit 6	Bit 2	Bit 6	Bit 2
Bit 5	Bit 1	Bit 5	Bit 1	Bit 5	Bit 1	Bit 5	Bit 1	Bit 5	Bit 1
Bit 4	LSB Bit 0	Bit 4	LSB Bit 0	Bit 4	LSB Bit 0	Bit 4	LSB Bit 0	Bit 4	LSB Bit 0

control board. The 8-bit data portion of the control word command represents eight 1-bit enables for the 8 CsI crystals associated with that pipe. The default value is enabled, data bit value '0'. Table 3 shows the relationship of the log ends to control words and bits. The orientation is the log end seen when facing a calorimeter side.

Referencing Figure 12, the following alignments are noted:

X+ Face, Control word 0 bit 7 aligns with readout log end number 00.

X- Face, Control word 0 bit 7 aligns with readout log end number C8.

Y+ Face, Control word 0 bit 7 aligns with readout log end number 49.

X+ Face, Control word 0 bit 7 aligns with readout log end number 81.

For example, to accept triggers from only the log end on the X+ side, top row, 3rd column from the left, Fig. 12 readout data word 10, requires the following commands to the calorimeter X+ control board.

0x10 0xFF // disable pipe 0 triggers and counters.

0x11 0x7F // disable pipe 1 except for MSB bit 7.

0x12 0xFF // disable pipe 2 triggers and counters.

0x13 0xFF // disable pipe 3 triggers and counters.

0x14 0xFF // disable pipe 4 triggers and counters.

3.3. DAC Programming Sequence (0x20 – 0x24)

Each Front End Electronics board contains 16 DACs to program ASIC discriminator levels, gain settings, and shaping time constants Two quad DAC devices provide four programmable DACs with 12-bit resolution over the voltage range 0 – 5.0 V. (Test DAC is 0 – 2.5 V.) Two quad DAC devices provide 10 DACs with 10-bit resolution over 0 – 5.0 V range. Table 4 defines the DAC functions and their addressing.

The 12-bit DACs are programmed thru two command functions: 0x20 – load dac high byte, and 0x21 or 0x22 – load dac0,1 low byte. In the

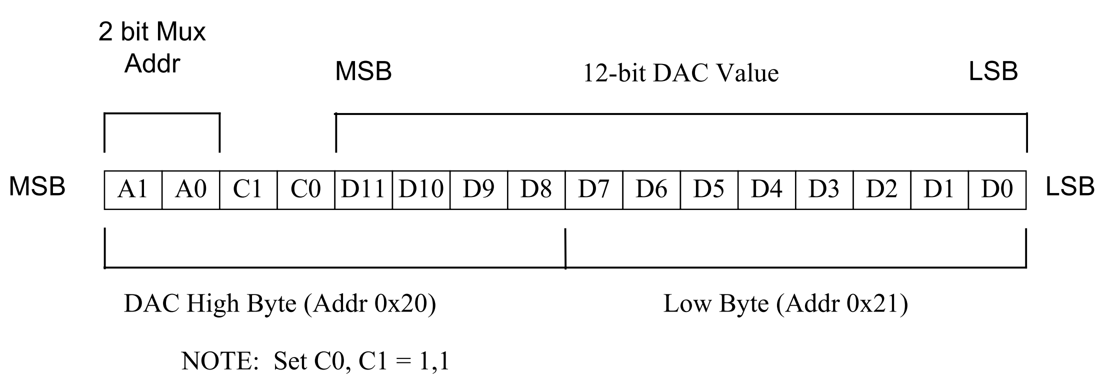

Figure 8. 16-bit DAC programming parameter for 12-bit DACs

Table 4. Definition of DAC Mnemonics and Addresses

DAC Mnemonic	Description	Low Byte DAC Addr	DAC Mux Addr	# bits	Vmax (V)
DLEX4	LowEn x4 LLD ref (REFLLD), 12 bit	0x21	0	12	5.0
DFLE	Fast LowEn LLD ref (REFHF), 12 bit	0x21	1	12	5.0
DUL	ULD ref (REFULD), 12 bit	0x21	2	12	5.0
DFHE	FAST HiEn LLD ref (REFLF), 12 bit	0x21	3	12	5.0
TEST	Test Pulse Amplitude (VTDC)	0x22	0	12	2.5
ICNTRL	Current Threshold, CsICal (ICNTRL)	0x22	1	12	5.0
VICNTRL	Current Threshold, VICal (IV_CNTRL)	0x22	2	12	5.0
SPARE	Spare	0x22	3	12	5.0
GFLES	Fast LowEn Shaper Gain Cntrl (VGCFH)	0x23	0	10	5.0
GHES	HiEn Shaper Gain Cntrl (VGCL)	0x23	1	10	5.0
GHEX8S	HiEn x8 Shaper Gain Cntrl (VGC8L)	0x23	2	10	5.0
GFHES	Fast HiEn Shaper Gain Cntrl (VGCFL)	0x23	3	10	5.0
FBPA	Preamp feedback cntrl (VFBPA)	0x24	0	10	5.0
FBSA	Shaping amp feedback cntrl (VFC)	0x24	1	10	5.0
GLES	LowEn Shaper Gain Cntrl (VGCH)	0x24	2	10	5.0
GLEX4S	LowEn x4 Shaper Gain Cntrl (VGC4H)	0x24	3	10	5.0

programming sequence, the high byte command must preceed the low byte specification. Figure 8 identifies the organization of the required 16-bit DAC parameter specification into the data fields of the dac high byte and dac low byte commands. The high byte identifies which DAC in the quad unit and the most significant 4 bits of the 12-bit DAC value. The low byte defines the least significant 8 bits of the value. Bits C0 and C1 in the high byte should be set to 1,1.

The 10-bit DACs are programmed thru the same command function for the high byte, 0x20 – load dac high byte, and one of three functions for the low byte, 0x23 – 0x24, load dac2 – dac3 low byte. In the programming sequence, the high byte command must preceed the low byte specification. Figure 9 identifies the organization of the required 16-bit DAC parameter specification into the data fields of the dac high byte and dac low byte commands. The high byte identifies which DAC in the quad unit and the most significant 4 bits of the 10-bit DAC value. The low byte defines the least significant 6 bits of the value. Note that the two LSBs of the low byte should be set to zero. Bits C0 and C1 in the high byte should be set to 1,1.

3.4. Event Data Readout Mode Programming (0x30)

NOTE: *For the BFEM, CAL TEM software has been modified to expect only four range*

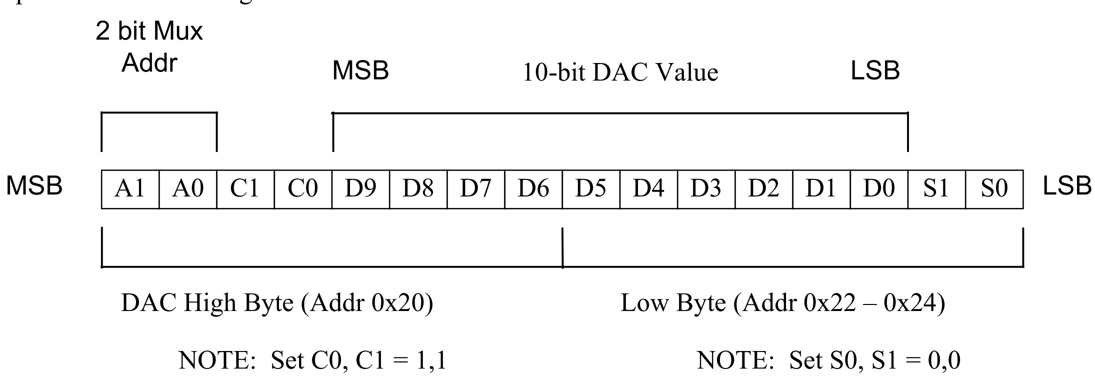

Figure 9. 16-bit DAC parameter for 10-bit DACs

Table 5. Data Readout Mode Bits

Data Readout Mode 4 Bit Value	Definition
0	Readout Low Energy Channel, x4 Gain
1	Readout Low Energy Channel, x1 Gain
2	Readout High Energy Channel, x8 Gain – Nominal
3	Readout High Energy Channel, x1 Gain - Nominal
4	Readout High Energy Chan, x8 Gain, - Test Gain (1pF preamp)
5	Readout High Energy Chan, x1 Gain, - Test Gain (1pF preamp)
6	Calibration Mode, Read all 4 Combinations (0,1,2,3)
7	Calibration Mode, Read all 4 Combinations (0,1,4,5)
8 - 13	Not normally used, same as 0 - 5
14	Calibration Mode, Generate TREQ and read all 4 Combinations (2,3,0,1)
15	Calibration Mode, Generate TREQ and read all 4 Combinations (4,5,0,1)

readouts, ie. data readout mode 6.

The calorimeter controllers support several selections for event data readout. The selection must be made prior to the level 1 triggers and is generally set once for an entire data run. There are two basic modes:

1. Readout all four gain ranges. In this mode there are four sequential readouts of the calorimeter, or, as described in section 1, 4×84 32-bit words. In this mode, there are four "sub-modes" which indicate whether the high energy channel should collect data with its test gain (hi gain mode) or its nominal gain. The other submodes control which of the energy ranges are readout first. See discussion below for the details. The test gain is useful for ground testing of the high energy channel using muons; it raises the gain of the high energy channel so that muons create a measureable signal. Also note that since there is no high energy trigger output, the high energy test injections always produce a trigger request irrespective of the LLD or Fast discriminator settings.
2. Readout a single gain range. In this mode a single gain range is selected for readout. A single readout of 84 32-bit words is assembled in the TEM.

The 4-bit data values to specify the readout mode for the event readout mode command are listed in Table 5. Modes 6,7,14 and 15 specify various calibration readout modes that readout all four energy ranges. In this mode the readout appears as four events with identical event Ids. Energy range bits are encoded in the least significant 2 bits of each ADC value. As described in Table 5, these four modes include selection of test gains for the high energy range and readout sequence for the low and high gain channels. This ordering is important for test charge injection (see 3.6 below), since only the PIN associated with the 1st readout range receives the injected charge.

NOTE: *It is important that all four cal control boards are set to the same event readout mode. Otherwise the data handling software in the TEM will likely be confused and/or the TEM documentation of the event data will be incorrect or incomplete.*

3.5. Calorimeter Trigger Mode Programming (0x40)

The calorimeter control boards support two modes for generating calorimeter triggers which are sent out to the TEM card for incorporation into the level 1 trigger. The trigger mode should be programmed prior to the starting of level 1 triggers. The trigger mode is programmed by a 2-bit data field in the trigger mode command. The specifications of this field and the associated

Table 6. Trigger Mode Specification

Trigger Mode 2 Bit Value	Defintion
0,1,2	Trigger on at least one hit in any row. (LowEn Fast)
3	LLD Muon Trigger (LowEnx4 LLD, 3.5 usec shaped)

trigger mode are identified in Table 6.

NOTE: *It is important that all four cal control boards are set to the same trigger mode. Otherwise the TEM documentation of the event data will be incorrect or incomplete.*

~~3.6 Trigger Information Requests (0x50 and 0x51)~~

~~After the occurance of a trigger, trigger information request commands can be used to determine the detectors which generated the trigger. The information is returned in the command response data field in place of the 8-bit command status field. The definition of the responses are identified in Table 7. The 0x50 command interrogates trigger register 0 and the command, 0x51 interrogates register 1. The layers identified in the table are sequenced from top to bottom. For the X+ and X- sides, the sequence numbers represent layers 0,2,4,6; for the Y+ sides, the sequence numbers represent layers 1,3,5,7. (See section 1.)~~

3.6. Test Charge Injection Request (0x60)

The calorimeter FEE boards provide test pulse generation for calibration and functionality testing. The test pulses are generated by first setting a pulse amplitude by setting a DAC value. The command, test charge injection request, then pulses that voltage into the test inputs to the FEE ASIC preamps. NOTE: Only one of the LowEn and HiEn preamps see the injected charge. The one that receives the charge is determined by the event readout mode pre-selected as described in section 3.4. For Event readout modes 0,1,6, and 7 the LowEn preamp receives the charge; for modes 2,3,4,5,14, and 15 the HiEn preamp receives the charge. The LowEn preamp is sees the injected charge on a 1 pF capacitor; the HiEn preamp is coupled with a 15 pF capacitor. There is one test charge injection per command.

NOTE: The test charge is injected into only one calorimeter controller at a time so that it is impossible to excite all four controllers in the same event.

3.7. Pedestal Baseline Trigger Request (0x61)

Causes a calorimeter trigger request without injecting a charge. One trigger occurs per command.

3.8. Readout Dead Time (0x70)

A programmable register is available to increase the readout dead time beyond the end of the readout cycle. This may be needed to keep the readout-generated noise from triggering the discriminators. Scaling for the dead-time data word is 200 nsec per bit. The default value is the maximum extra deadtime, 255×200 nsec/bit = 51 μsec.

3.9. Counter Dead Time (0x71)

A programmable single bit register is available to enable event counting during the event data readout cycle. The default counter dead time consists of the sum of three parts:

1) Counter “digital monostable” time.

2) Event data readout time.

3) Counter readout time.

The “digital monostable” process shares a digital timer between all triggers on one side of a calorimeter. Upon first detecting a trigger edge, this shared timer is started. All counters are enabled to count the first edge transition for a discriminator. At 3.2 μsec, all counters are disabled from counting. At 6.4 μsec if the event data readout process has started and the Counter

Table 7. Trigger information bits

Bit Position	Reg 0 - Row – Description	Reg 1 – Col – Description
0 LSB	Row 0 (Top) “or”	Column 2 “or”
1	Row 1 “or”	Column 3 “or”
2	Row 2 “or”	Column 4 “or”
3	Row 4 (Bottom) “or”	Column 5 “or”
4	Adj side Row 0 “or”	Column 6 “or”
5	Adj side Row 1 “or”	Column 7 “or”
6	Column 0 “or”	Column 8 “or”
7	Column 1 “or”	Column 9 “or”

Deadtime bit (0x71) has not been set, then the shared timer halts until the readout is completed. Upon the timer reaching 10 μsec, the timer is reset, ready to repeat the process. If a commanded event data readout occurs without the discriminator transition detection, the shared timer is started and the same execution is followed.

3.10. Resetting of the Calorimeter Controller Board.

The cal controller board reloads its Xilinx FPGA program upon Reset signal being asserted by the TEM. The cal controller is then in its initial power up state. Note that the calorimeter FEE boards DACs retain their current value through the reset process.

4. Calorimeter Command Scripting and Parsing

The commanding of the Calorimeter shall be supported by an ASCII command script parsing method which will permit "user-friendly" alphanumeric specification of commands without having to resort to the hexidecimal values for the commands. These ASCII command strings may be typed-in individually or be piped from a script file. The parsing language shall have the following features:

1. Enabling/disabling a log file of command requests and responses
2. Setting the default subsystem (eg. CAL, ACD, TKR, etc) for subsequent commands. On initialization, the subsystem is assumed to be CAL. At this time, the code will only support CAL commanding.
3. Setting the default calorimeter controller mux address for subsequent commands
4. Parsing commands of the form: <subsystem> <calmuxcode> <cmdmnem> <cmddatavalue> <; optional comments>, for example

```
CAL X+ DAC LowEnx4 100.0  ;
set threshold to 100 mv
```

   Both of the <subsystem> and <calmuxcode> may be omitted. In that case, the default values for those parameters will be inserted in the command. The default values are defined using a "SET" command.

NOTE: If a command specifies the <subsystem> or <calmuxcode> prefix, this value becomes the default for all subsequent commanding until changed again by another prefix or by the SET commands.

Commands to the calorimeter shall be sent as 32-bit binary codes. The least significant 16 bits contain the 16-bit command function and associated data as described in section 3. The most significant 16-bits specify the calorimeter control card and subsystem (eg. CAL). This is shown in Figure 10.

The commands to the Cal TEM are allocated command function opcodes in the calorimeter controller command space. These commands have opcodes in the range 0xF0 – 0xF1. These command opcodes will be trapped in the TEM and not passed on to the calorimeter controllers. Similarly, the TEM command processor will guarantee that all four cal controllers operate in the same event data mode and trigger mode by sending any received command with those opcodes to all four controllers.

MSByte LSByte

SubSysID	CalMuxID	16-bit Command
8-bit	8-bit	16-bit

Figure 10. 32-bit format of Commands to the TEM command processor. SubsysID identifies CAL command and is zero. The least significant two bits of CalMuxID field set the cal control board mux.

Table 8. Calorimeter Command Mnemonics – Command Parsing Environment

Command	Modifier	Data	Comment
SET	SUBSYSTEM	CAL	Subsequent commands go to calorimeter. This is initialized default
		{ACD, TKR, …}	Alternate subsystem specs
SET	CALMUX	{X+, Y+, X-, Y-, 0 - 3}	Set the command mux to the specified control board. Subsequent commands without calmuxcode will use this spec
SET	LOGFILE	<filename>	Close any open logfile and open new log as file <filename>
SET	LOGFILE	OFF	Close any open logfile (obviously, can't create logfile named OFF)

Table 9. Calorimeter Command Mnemonics - TEM Configuration

Command	Modifier	Data	Comment
RESET	None	None	Performs TEM card reset of calorimeter controllers and FIFOs. Use pseudo Cmdfunc = 0xF0
RESET	FIFO	None	Performs TEM card reset of FIFO and TEM FPGAs only. Use pseudo Cmdfunc = 0xF1
RESET	TRIGCNT	None	Performs TEM card reset of trigger counter register. Use pseudo Cmdfunc = 0xF2
L1T		{ON, OFF}	Enable/disable TEM recognition of Level 1 trigger inputs. Use pseudo Cmdfunc = 0xF3
CTREQ		{ON, OFF, 0x0 – 0xF)	Enable, disable or selectively enable the cal trigger req from the four controller cards. Hex values 0x0 – 0xF mask sides individually. ON = 0x0, OFF = 0xf. These are mask bits. Use pseudo Cmdfunc = 0xF4
STARTBIT		{X+,Y+, X-,Y-, 0 - 3}	Sets the TEM startbit mux to the specified controller card. Use pseudo Cmdfunc = 0xF5
CMUX		{X+, Y+,X-,Y-, 0 - 3}	Sets the TEM command mux to the specified controller card. Use pseudo Cmdfunc = 0xF6. Not normally used. Calmux setting (0xF6) will precede all parsed commands which address a specific controller

Table 10. Calorimeter Command Parsing - Commands to the Cal Controllers

Command	Modifier	Data	Comment
RATES			Readout rates from specified controller. Cmdfunc = 0x00. NOTE: this is useful for test only. TEM process normally acquires and transmits rates at fixed frequency.
CONTROL	<pipeid=0-4>	{0x00 – 0xFF)	8 1-bit trigger discriminator enables. (also enables singles rate counting) Cmdfunc = 0x10 – 0x14 MSB controls ASIC0, LSB for ASIC7 of pipe
DAC	{<dacmnem>, 0 – 15} See Table 4 for the mnem. Definitions	Dac value in millivolts or hex setting (0xnnn) Or level (Nnnnn)	Set specified dac to value. Creates correct sequence of 0x20 – 0x24 cmds.
EVENT		{0 - 15}	Set event data readout mode. Cmdfunc = 0x30. NOTE: TEM software sends this same command to all four controllers.
TRIGGER		{0,2,3}	Set trigger generation mode. Cmdfunc = 0x40. NOTE: TEM software sends this same command to all four controllers.
INFO		<register id, 0, 1)	Get the trigger information bits on last trigger from specified controller: Cmdfunc = 0x50, 0x51 NOTE: this is useful for test only.
PULSE		<number of pulses, {0 – 255}	Inject a test charge pulse for the specified controller. Cmdfunc 0x60. Optional specification of number of pulses in data field. If not present, inject one pulse. TEM software will repetitively inject pulses at 1 ms intervals for the specified number.
PEDESTAL		<number of pulses, {0 – 255}	Create single trigger without injecting test charge for the specified controller. Cmdfunc 0x61.

5. BFEM Calorimeter Commanding

For the balloon flight, the full commanding functionality shall be available only via hard wire access during ground test and checkout. During the balloon flight, commanding of the calorimeter shall be limited to the execution of preloaded command macros that potentially configure many command functions.

The needed command macros are described below.

5.1. Default Configuration

This macro is executed at power on and by command when the desire is to place the calorimeter into a known, safe state with cal trigger requests disabled.

This macro sets the bias and discriminator DACs to nominal operating values, enables the individual crystal inputs to the trigger logic, sets the default trigger and event readout modes, and exits with the cal trigger requests disabled.

There could be several standard configurations that are selected using this macro and a single modifying parameter to identify which configuration to use.

5.2. Fast Trigger Mode

This macro changes the calorimeter trigger mode to the Fast LE discriminator logic.

5.3. LEX4 Trigger Mode

This macro changes the calorimeter trigger mode to the LEX4 discriminator logic.

5.4. Set LEX4 Discriminators

This macro sets all LEX4 Discriminators to the value associated with the single parameter input to the macro. The value is set in the appropriate DAC for all four sides.

5.5. Set FLE Discriminators

This macro sets all FLE Discriminators to the value associated with the single parameter input to the macro. The value is set in the appropriate DAC for all four sides.

5.6. Disable Crystal Discriminator

This command permits the individual disabling of each crystal end. The crystal and end are identified in the parameter to the macro. There are 160 crystal ends to encode.

The purpose of this command is to remove noisy discriminators from the cal trigger request logic to stop excessive trigger requests.

5.7. Enable Crystal Discriminator

This command permits the individual enabling of each crystal end. The crystal and end are identified in the parameter to the macro. There are 160 crystal ends to encode.

5.8. Calorimeter Reset

This command function resets the cal controller without clearing the DAC contents. It could be used in conjunction with FIFO resets and event ID clearing.

Perhaps these functions are already part of a global BFEM reset operation and are not needed here.

6. Level 1 Trigger Support

6.1. Calorimeter Trigger Generation

The TEM board has 4 differential inputs reserved for trigger requests from the calorimeter(Cal Req), and will generate a single calorimeter tower trigger (Level 1 Trigger) when any of the four input triggers are asserted. All trigger lines are asserted low. The calorimeter controller boards, individually, perform the logic required for determining a Cal Request trigger depending on the trigger mode selection (see section 3.5). The Cal Request trigger should be generated within 200 nsec of an event occuring and will be of minimum of 200 nsec in width. The maximum width of the Cal Request trigger is the time-over-threshold of the analog signal. Additional information on the last calorimeter trigger request is obtained by using the Trigger Information command.

NOTE: *If the calorimeter trigger mode is set to the ground test configuration (3) for triggering on muons on the LowEn x4 LLD, the CalReq cannot be assured within the 200-nsec spec above. The slow shaping of the signal precludes that possibility. The CalReq in that configuration could be delayed by as much as 3.5 μsec*

NOTE: *While the V2 TEM board supports both Cal High and Cal Low trigger requests, the prototype calorimeter controllers only support the Cal Low trigger. There are no connections to the Cal Hi trigger request lines.*

```
> ; everything after the semicolon is comment
> ; parser is not case sensitive - upper and lower case are the same.
> set logfile mylog990728.log   ; turns on logging to specified file
> set subsys cal                ; sets default subsystem to calorimeter
> reset                         ; resets the calorimeter controller
> cal reset                     ; same as above but with subsystem identified
> X+ dac FLE  100.0             ; set X+ fast low energy threshold to 100 mV
> set calmux X+                 ; default controller is X+
> dac FLE 100.0                 ; set X+ fast low energy thresh to 100 mV
> dac FLE 0x100                 ; set X+ fast low en thresh to level 100 hex.
> dac pulse 500.0               ; set dac for test pulse amplitude to 500 mV
> pulse  1                      ; inject 1 test pulse into all controllers
> pulse   100                   ; inject 100 test pulses at 16 msec intervals.
```

Figure 11. Example Command Script.

6.2. GLAST Level 1 Trigger:

The TEM board will have 4 differential outputs to communicate to each calorimeter side that a Level 1 Trigger event has occurred. The TEM board will generate a Level 1 Trigger within 500 nsec of receiving a calorimeter tower trigger. The Level 1 Trigger will then iniate calorimeter data readout.

NOTE: *The four calorimeter control boards must receive the Level 1 Trigger signal simultaneaously as determined by its detection on all four boards by the rising edge of the same 20 MHz clock pulse. If this simultaneity is not met, the 20 serial event readout will not be correctly phased and the TEM assembly of the event data will be corrrrupted corrupted.*

7. Calorimeter Readout Organization:

The readout of all 4 sides of the calorimeter will be arranged in a manner to simplify the processing of data by dowstream processors.

7.1. Calorimeter Coordinate System.

The Calorimeter has readout electronics on all four side faces. Opposing sides readout the two ends of the same CsI logs. The coordinate system for calorimeter readout discussions is the following:

Table 11. Coordinate System Definition

Z-Axis:	Points outward to the on-axis target position ("the viewing direction"), normal to the plane formed by the top layer of calorimeter logs
X-Axis:	At this point, arbitrary. By definition, the top layer of logs in the calorimeter have their long dimension parallel with this axis.
Y-Axis:	At this point, arbitrary, but forming "right-handed" coordinate system with X & Z. On the S/C it is likely to be aligned with the solar panel rotation axis

7.2. CsI Event Data Readout

The event data readout is organized by side face. Each side face supports the readout of 40 CsI log ends. The Front-End Electronics (FEE) control reads out the data in 5 "Pipes" per side. Each Pipe handles 8 ADC values which are readout in defined sequence, as shown in Figure 3. The sequence and sequence number encoded in the 16-bit data value per ADC as shown in Table 6.

The faces of the calorimeter are identified by a two-character coordinate of the face: X+, Y+, X–, and Y–. (Also identified as 0,1,2, and 3, respectively.) The X+ electronics, for example, reads out the ends of the logs, aligned along the X- axis, at their +X end.

The data are readout in columnar sequence always starting at the top (+Z) and working to the bottom. The columns are readout from the "negative edge" to the "positive edge". That is, the X+,X– faces readout from the edge in the Y– direction to the Y+ edge, and the Y+, Y– faces readout from the edge in the X– direction to the X+ direction. This readout sequence is reflected in the numbering scheme for the CsI log ends which is defined in Table 13 and shown graphically in Figure 12. The log end and ADC is identified by 8-bit Hex value. The most significant bit identifies the log end (0 = + face, 1 = – face).

The readout sequence for the four faces of the calorimeter is identified in Table 13. Refer to Figure 12 for geometric arrangement of the ADC Ids. In general, the faces readout from top to bottom but the column order is different for the faces. For the X+ face and the Y- face, the columns readout from left to right. For the X- face and the Y+ face, the columns readout from right to left. This ordering permits the assembly of the ADC values from the two ends of each CsI log into a single 32-bit word. This ordering is achieved first in the calorimeter controller by reading the 8 ADCs in the five pipes in the correct order, and then by the TEM FPGA accessing the data from the 20 pipes (5 pipes per side of the calorimeter in the correct order). The pipes are numbered from left to right on the FEE cards and reflect the connector number to the cal controller card.

Table 12. Organization of Event Data from FPGA. Sixteen bits per log end.

MSBit			LSBit
ADC Value 12 Bits	ADC ID 2 bits	PIN ID 1 Bit	Range Scale 1 Bit
	Sequence # mod 4	0 = Big Pin 1 = Sml Pin	0 = amplified rng 1 = full scale

Table 13. ADC Readout Order for Event Data

Pipe ID	Seq No.	Event Readout ADC ID			
		X+ Face	Y- Face	X- Face	Y+ Face
0	0	00	81	C0	41
	1	02	83	C2	43
	2	04	85	C4	45
	3	06	87	C6	47
	4	08	89	C8	49
	5	0A	8B	CA	4B
	6	0C	8D	CC	4D
	7	0E	8F	CE	4F
1	0	10	91	B0	31
	1	12	93	B2	33
	2	14	95	B4	35
	3	16	97	B6	37
	4	18	99	B8	39
	5	1A	9B	BA	3B
	6	1C	9D	BC	3D
	7	1E	9F	BE	3F
2	0	20	A1	A0	21
	1	22	A3	A2	23
	2	24	A5	A4	25
	3	26	A7	A6	27
	4	28	A9	A8	29
	5	2A	AB	AA	2B
	6	2C	AD	AC	2D
	7	2E	AF	AE	2F
3	0	30	B1	90	11
	1	32	B3	92	13
	2	34	B5	94	15
	3	36	B7	96	17
	4	38	B9	98	19
	5	3A	BB	9A	1B
	6	3C	BD	9C	1D
	7	3E	BF	9E	1F
4	0	40	C1	80	01
	1	42	C3	82	03
	2	44	C5	84	05
	3	46	C7	86	07
	4	48	C9	88	09
	5	4A	CB	8A	0B
	6	4C	CD	8C	0D
	7	4E	CF	8E	0F

The TEM shall assemble the 20 pipes into a data message of 81 32-bit words. The word ordering and content are described in Table 14 below. In the calorimeter readout mode in which all four energy ranges are readout, they appear as four sequential messages of the format in Table 14 with identical 32-bit Event ID in word 0. The messages appear in the order: LowEn x4, LowEn, HiEn x8, Hi En.

NOTE: *The BFEM TEM card now implements this order. Previously, calorimeter software executing in the TEM PPC reordered the FIFO data to achieve this ordering.*

Table 14. ADC Readout Order in TEM 84 Word Event Message

Seq No.	32-bit Word Content		Data Source[*]	
	High 16-bit	Low 16-bit	High 16-bit	Low 16-bit
0	32-bit Event ID		TEM Event Counter	
1	32-bit Timer Word		TEM Event Trigger Time	
2	32-bit TREQ/VETO status		TEM Event Treq/Veto/Status	
3	ADC 00	ADC 80	X+, 0, 0	X-, 4, 0
4	ADC 10	ADC 90	X+, 1, 0	X-, 3, 0
5	ADC 20	ADC A0	X+, 2, 0	X-, 2, 0
6	ADC 30	ADC B0	X+, 3, 0	X-, 1, 0
7	ADC 40	ADC C0	X+, 4, 0	X-, 0, 0
8	ADC 01	ADC 81	Y+, 4, 0	Y-, 0, 0
9	ADC 11	ADC 91	Y+, 3, 0	Y-, 1, 0
10	ADC 21	ADC A1	Y+, 2, 0	Y-, 2, 0
11	ADC 31	ADC B1	Y+, 1, 0	Y-, 3, 0
12	ADC 41	ADC C1	Y+, 0, 0	Y-, 4, 0
13	ADC 02	ADC 82	X+, 0, 1	X-, 4, 1
14	ADC 12	ADC 92	X+, 1, 1	X-, 3, 1
15	ADC 22	ADC A2	X+, 2, 1	X-, 2, 1
16	ADC 32	ADC B2	X+, 3, 1	X-, 1, 1
17	ADC 42	ADC C2	X+, 4, 1	X-, 0, 1
18	ADC 03	ADC 83	Y+, 4, 1	Y-, 0, 1
19	ADC 13	ADC 93	Y+, 3, 1	Y-, 1, 1
20	ADC 23	ADC A3	Y+, 2, 1	Y-, 2, 1
21	ADC 33	ADC B3	Y+, 1, 1	Y-, 3, 1
22	ADC 43	ADC C3	Y+, 0, 1	Y-, 4, 1
23	ADC 04	ADC 84	X+, 0, 1	X-, 4, 1
24	ADC 14	ADC 94	X+, 1, 1	X-, 3, 1
25	ADC 24	ADC A4	X+, 2, 1	X-, 2, 1
26	ADC 34	ADC B4	X+, 3, 1	X-, 1, 1
27	ADC 44	ADC C4	X+, 4, 1	X-, 0, 1
28	ADC 05	ADC 85	Y+, 4, 1	Y-, 0, 1
…….	…….	…….	…….	…….
70	ADC 2D	ADC AD	Y+, 2, 6	Y-, 2, 6
71	ADC 3D	ADC BD	Y+, 1, 6	Y-, 3, 6
72	ADC 4D	ADC CD	Y+, 0, 6	Y-, 4, 6
73	ADC 0E	ADC 8E	X+, 0, 7	X-, 4, 7
74	ADC 1E	ADC 9E	X+, 1, 7	X-, 3, 7
75	ADC 2E	ADC AE	X+, 2, 7	X-, 2, 7
76	ADC 3E	ADC BE	X+, 3, 7	X-, 1, 7
77	ADC 4E	ADC CE	X+, 4, 7	X-, 0, 7
78	ADC 0F	ADC 8F	Y+, 4, 7	Y-, 0, 7
79	ADC 1F	ADC 9F	Y+, 3, 7	Y-, 1, 7
80	ADC 2F	ADC AF	Y+, 2, 7	Y-, 2, 7
81	ADC 3F	ADC BF	Y+, 1, 7	Y-, 3, 7
82	ADC 4F	ADC CF	Y+, 0, 7	Y-, 4, 7
83	32-bit Dead cause/time		TEM Event Dead cause/time	

[*] The data source is identified as side (eg. X+), pipe id, and ADC sequence in that pipe.

TEM STAT/TREQ/VETO Word:

Bit	Definition
12	Cal Readout mode 640/160, High = 640
11	Readout busy: Max (High, non-pipelined), Min (Low, pipelined)
10	ACDL Veto
9	CPU TREQ
8	EXT TREQ
7	CAL TREQH 3
6	CAL TREQH 2
5	CAL TREQH 1
4	CAL TREQH 0
3	CAL TREQL 3
2	CAL TREQL 2
1	CAL TREQL 1
0	CAL TREQL 0

TEM Dead Time Cause/Dead Time Word:

Bit	Definition
17	Readout L1T Wait
16	CPU Busy
15	Data FIFO Full
14	Cal Readout Busy
13 - 0	Dead Time Counter (50 nsec)

***NOTE**: In calorimeter readout mode of all four ranges (640), only the last range readout has correct deadtime information.*

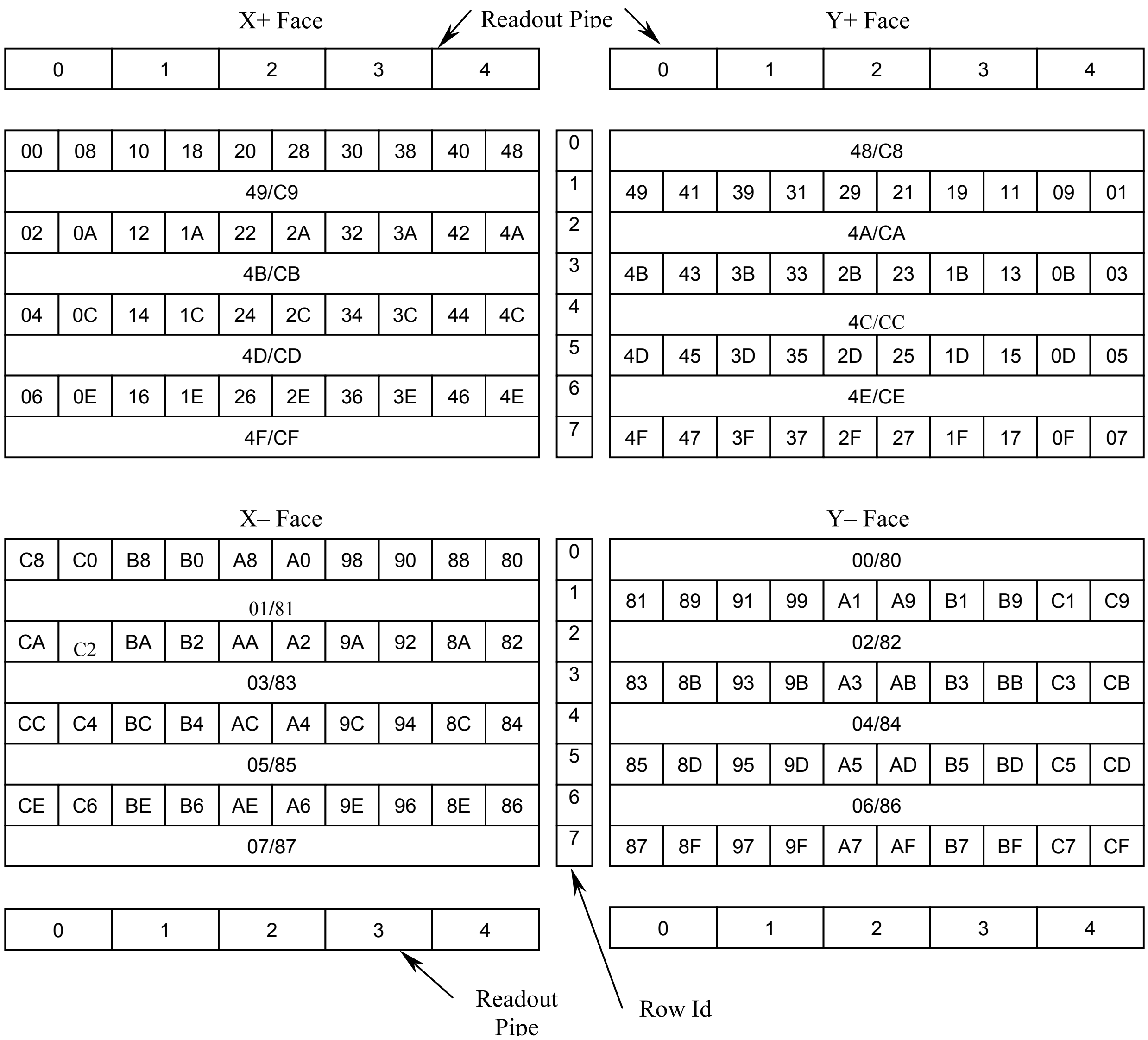

Figure 12. Graphical display of CsI log end enumeration. CsI crystal readouts are identified by 8-bit hex code. The most significant bit is the log-end identifier; thus code 00 and 80 identify the two ends of the same log.

8. Housekeeping Rate Readout Organization

~~Each crystal end LEX4 discriminator has a rate counter associated with it~~.

For the balloon flight, the CAL housekeeping rates monitor the FLE discriminators for each of the crystal ends. These rate counters are readout using the rate housekeeping command function, 0x00. Note that the rate command must be executed for each of the four sides of the calorimeter. The integration time for the rate measurements is determined by solely by the time interval between successive rate readout commands. On readout command, the count is frozen, transferred to an output buffer; the counter is zeroed and counting resumes. Each counter is a 16-bit value with maximum count of 65535 per sample.

The deadtime for the counter is the "or" of two components. 1) The counters are dead during a L1T digitization. 2) Each discriminator firing has a fixed deadtime of (TBM) μs.

In the BTEM software a separate housekeeping process controlled the rate housekeeping readout. Every ten seconds it would wakeup and readout the four sides of the calorimeter. The readout consisted of the concatenation of the four individual sides, ie. the first 40 16-bit values were from the X+ side, then the Y+ side, X- side, and finally the Y- side. The crystal Ids for the 40 element reads is identified in Table 15. A header consisting of timestamp, version number, and block size was prepended to the counter readouts in the message.

Table 15. Definition of Rate Counters

Counter Number	Readout address	Rate Counter from Low En x4 Discriminator for CsI Log ID#			
		X+ Side	X- Side	Y+ Side	Y- Side
0	0x0104	00	C8	49	81
1	0x0108	08	C0	41	89
2	0x010C	02	CA	4B	83
3	0x0110	0A	C2	43	8B
4	0x0114	04	CC	4D	85
5	0x0118	0C	C4	45	8D
6	0x011C	06	CE	4F	87
7	0x0120	0E	C6	47	8F
8	0x0124	10	B8	39	91
9	0x0128	18	B0	31	99
10	0x012C	12	BA	3B	93
11	0x0130	1A	B2	33	9B
12	0x0134	14	BC	3D	95
13	0x0138	1C	B4	35	9D
14	0x013C	16	BE	3F	97
15	0x0140	1E	B6	37	9F
16	0x0144	20	A8	29	A1
17	0x0148	28	A0	21	A9
18	0x014C	22	AA	2B	A3
19	0x0150	2A	A2	23	AB
20	0x0154	24	AC	2D	A5
21	0x0158	2C	A4	25	AD
22	0x015C	26	AE	2F	A7
23	0x0160	2E	A6	27	AF
24	0x0164	30	98	19	B1
25	0x0168	38	90	11	B9
26	0x016C	32	9A	1B	B3
27	0x0170	3A	92	13	BB
28	0x0174	34	9C	1D	B5
29	0x0178	3C	94	15	BD
30	0x017C	36	9E	1F	B7
31	0x0180	3E	96	17	BF
32	0x0184	40	88	09	C1
33	0x0188	48	80	01	C9
34	0x018C	42	8A	0B	C3
35	0x0190	4A	82	03	CB
36	0x0194	44	8C	0D	C5
37	0x0198	4C	84	05	CD
38	0x019C	46	8E	0F	C7
39	0x01A0	4E	86	07	CF

Appendix A. BFEM CAL Interconnections with TEM.

The main signal communications between the TEM and one calorimeter control is shown pictorially in Figure 13. The TEM connects to four calorimeter control boards.

Communication of all signals is performed with Low Voltage Differential Signaling (LVDS). LVDS transmitters signal bits by changing the direction of a small output current. The LVDS receiver detects the change in voltage polarity across a resistor matched to the line. A common connector pin out is used between each of the Calorimeter Control Boards and the Calorimeter TEM Board. Note that the TEM board does not supply power to the Calorimeter.

The cable signal connections are shown in Table 16.

Table 16. Signal connections between TEM and Calorimeter

TEM Pin #	Cal Pin #	Description
	37	+5V
	36	+5V
	35	+5V
	34	+5V
	33	+PIN_Bias Voltage
	32	Bias Return
	31	Gnd
	30	Gnd
	29	Gnd
	28	Gnd
	27	Gnd
12	26	Data0_Hi
13	25	Data0_Lo
14	24	Data1_Hi
15	23	Data1_Lo
16	22	Data2_Hi
17	21	Data2_Lo
18	20	Data3_Hi
19	19	Data3_Lo

TEM Pin #	Cal Pin #	Description
20	18	Data4_Hi
21	17	Data4_Lo
22	16	Cal_Busy_Hi
23	15	Cal_Busy_Lo
24	14	CalReq_Hi
25	13	CalReq_Lo
26	12	Level1_Trig_Lo
27	11	Level1_Trig_Hi
28	10	Clk_Lo
29	9	Clk_Hi
30	8	Cmd_Lo
31	7	Cmd_Hi
32	6	HskpDat_Lo
33	5	HskpDat_Hi
34	4	Reset_Lo
35	3	Reset_Hi
	2	Gnd
	1	Gnd

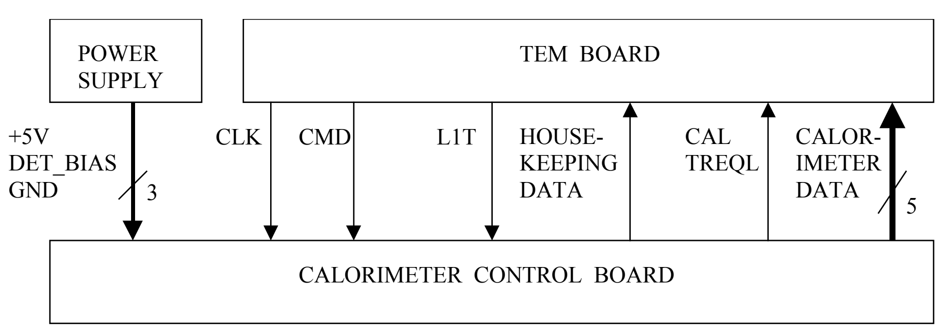

Figure 13 TEM – Calorimeter Signals

Appendix B. BTEM Calorimeter Command Configuration

The calorimeter was configured for the beam test using scripts executed on the CalGSE. The main script was cal_setup.cmd. It references another script dac_setup.cmd. The net result of the scripts is to cycle thru the four sides of the calorimeter setting dac values and discriminator enables. In this script, all four sides are set to the same configuration. The two scripts are listed below.

The commands generated by the script are also shown below in the log file. Generated command values are 4 byte hex numbers. Note that each dac setting command script actually results in two command values.

Cal setup.cmd

```
; setup calorimeter
; all sides the same and defined by dac_setup.cmd

ctreq off
set calmux 0
@dac_setup.cmd

set calmux 1
@dac_setup.cmd

set calmux 2
@dac_setup.cmd

set calmux 3
@dac_setup.cmd

event 6              ;set event mode to 6  - normal 4 range readout
trigger  3     ;set trigger mode to 3 - any row lex4

ctreq on
```

dac setup.cmd

```
; dac_startup.cmd from ossepd.nrl.navy.mil
; initialize the dac values

dac  dlex4    3750.0
dac  dfle     3593.8
dac  dul       444.3
dac  dfhe      444.3
dac  test       58.6
dac  icntrl    937.5
dac  vicntrl   312.5
dac  spare    2495.1
dac  gfles    2495.1
dac  ghes     3125.0
dac  ghex8s   4062.5
dac  gfhes    2495.1
```

```
dac  fbpa     3500.0
dac  fbsa      500.0
dac  gles     3125.0
dac  glex4s   4062.5

control 0 0x0 ; set control words for the 5 pipes
control 1 0x0
control 2 0x0
control 3 0x0
control 4 0x0

event 0             ;set event mode to 0
trigger  3     ;set trigger mode to 3
```

Log file from execution of command script

```
> @cal_setup.cmd
> ; setup calorimeter
> ; all sides the same
> ctreq off
  0000f400
> set calmux 0
> @dac_setup.cmd
> ; dac_startup.cmd from ossepd.nrl.navy.mil
> ; initialize the dac values
> dac  dlex4    3750.0
  0000203c
  00002100
> dac  dfle     3593.8
  0000207b
  00002180
> dac  dul       444.3
  000020b1
  0000216c
> dac  dfhe      444.3
  000020f1
  0000216c
> dac  test       58.6
  00002030
  00002230
> dac  icntrl    937.5
  00002073
  00002200
> dac  vicntrl   312.5
  000020b1
  00002200
> dac  spare    2495.1
  000020f7
  000022fc
> dac  gfles    2495.1
  00002037
  000023fc
> dac  ghes     3125.0
  0000207a
```

```
  00002300
> dac  ghex8s   4062.5
  000020bd
  00002300
> dac  gfhes    2495.1
  000020f7
  000023fc
> dac  fbpa     3500.0
  0000203b
  00002430
> dac  fbsa      500.0
  00002071
  00002498
> dac  gles     3125.0
  000020ba
  00002400
> dac  glex4s   4062.5
  000020fd
  00002400
> control 0 0x0 ; set control words for the 5 pipes
  00001000
> control 1 0x0
  00001100
> control 2 0x0
  00001200
> control 3 0x0
  00001300
> control 4 0x0
  00001400
> event 0            ;set event mode to 0
  00003000
> trigger  3     ;set trigger mode to 3
  00004003
> set calmux 1
> @dac_setup.cmd
> ; dac_startup.cmd from ossepd.nrl.navy.mil
> ; initialize the dac values
> dac  dlex4    3750.0
  0001203c
  00012100
> dac  dfle     3593.8
  0001207b
  00012180
> dac  dul       444.3
  000120b1
  0001216c
> dac  dfhe      444.3
  000120f1
  0001216c
> dac  test       58.6
  00012030
  00012230
> dac  icntrl    937.5
  00012073
  00012200
> dac  vicntrl   312.5
  000120b1
```

```
  00012200
> dac  spare    2495.1
  000120f7
  000122fc
> dac  gfles    2495.1
  00012037
  000123fc
> dac  ghes     3125.0
  0001207a
  00012300
> dac  ghex8s   4062.5
  000120bd
  00012300
> dac  gfhes    2495.1
  000120f7
  000123fc
> dac  fbpa     3500.0
  0001203b
  00012430
> dac  fbsa      500.0
  00012071
  00012498
> dac  gles     3125.0
  000120ba
  00012400
> dac  glex4s   4062.5
  000120fd
  00012400
> control 0 0x0 ; set control words for the 5 pipes
  00011000
> control 1 0x0
  00011100
> control 2 0x0
  00011200
> control 3 0x0
  00011300
> control 4 0x0
  00011400
> event 0             ;set event mode to 0
  00013000
> trigger  3     ;set trigger mode to 3
  00014003
> set calmux 2
> @dac_setup.cmd
> ; dac_startup.cmd from ossepd.nrl.navy.mil
> ; initialize the dac values
> dac  dlex4    3750.0
  0002203c
  00022100
> dac  dfle     3593.8
  0002207b
  00022180
> dac  dul       444.3
  000220b1
  0002216c
> dac  dfhe      444.3
  000220f1
```

```
  0002216c
> dac  test       58.6
  00022030
  00022230
> dac  icntrl    937.5
  00022073
  00022200
> dac  vicntrl   312.5
  000220b1
  00022200
> dac  spare    2495.1
  000220f7
  000222fc
> dac  gfles    2495.1
  00022037
  000223fc
> dac  ghes     3125.0
  0002207a
  00022300
> dac  ghex8s   4062.5
  000220bd
  00022300
> dac  gfhes    2495.1
  000220f7
  000223fc
> dac  fbpa     3500.0
  0002203b
  00022430
> dac  fbsa      500.0
  00022071
  00022498
> dac  gles     3125.0
  000220ba
  00022400
> dac  glex4s   4062.5
  000220fd
  00022400
> control 0 0x0 ; set control words for the 5 pipes
  00021000
> control 1 0x0
  00021100
> control 2 0x0
  00021200
> control 3 0x0
  00021300
> control 4 0x0
  00021400
> event 0            ;set event mode to 0
  00023000
> trigger  3     ;set trigger mode to 3
  00024003
> set calmux 3
> @dac_setup.cmd
> ; dac_startup.cmd from ossepd.nrl.navy.mil
> ; initialize the dac values
> dac  dlex4    3750.0
  0003203c
```

```
  00032100
> dac  dfle     3593.8
  0003207b
  00032180
> dac  dul       444.3
  000320b1
  0003216c
> dac  dfhe      444.3
  000320f1
  0003216c
> dac  test       58.6
  00032030
  00032230
> dac  icntrl    937.5
  00032073
  00032200
> dac  vicntrl   312.5
  000320b1
  00032200
> dac  spare    2495.1
  000320f7
  000322fc
> dac  gfles    2495.1
  00032037
  000323fc
> dac  ghes     3125.0
  0003207a
  00032300
> dac  ghex8s   4062.5
  000320bd
  00032300
> dac  gfhes    2495.1
  000320f7
  000323fc
> dac  fbpa     3500.0
  0003203b
  00032430
> dac  fbsa      500.0
  00032071
  00032498
> dac  gles     3125.0
  000320ba
  00032400
> dac  glex4s   4062.5
  000320fd
  00032400
> control 0 0x0 ; set control words for the 5 pipes
  00031000
> control 1 0x0
  00031100
> control 2 0x0
  00031200
> control 3 0x0
  00031300
> control 4 0x0
  00031400
> event 0            ;set event mode to 0
```

```
  00033000
> trigger  3     ;set trigger mode to 3
  00034003
> event 6            ;set event mode to 6  - normal 4 range readout
  00033006
> trigger  3     ;set trigger mode to 3 - any row     lex4
  00034003
> ctreq on
  0003f40f
```

TEM-CAL-VME2 Programming Guide
Board 1113-01-01C CAL READOUT FPGA Rev. 2.34

```
Board base address assumed to be 0x1000XXXX for use with Motorola Power PC VME board.

/* TEM CAL VME BOARD REGISTERS */

brdcntl=  0x0020              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE                                                                                                                    L      L      L
                               -      -      -      -      -     FPGA   FPGA   FPGA    -      -      -      -      -     RST    RST    RST
                                                                 DCLK   NCFG   SDAT                                        CAL    FIFO   FPGA


brdstat=  0x0030              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ                                                                                                                L      H
                               -      -      -      -      -      -      -      -      -      -      -      -     FPGA   FPGA    -      -
                                                                                                                   NSTAT  CFG
                                                                                                                   ERR    DONE

                              D31    D30    D29    D28    D27    D26    D25    D24    D23    D22    D21    D20    D19    D18    D17    D16
                               H      L      L      L      H      L      L      L      H      L      L      L      H      L      L      L
                              CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL
                              FIFO3  FIFO3  FIFO3  FIFO3  FIFO2  FIFO2  FIFO2  FIFO2  FIFO1  FIFO1  FIFO1  FIFO1  FIFO0  FIFO0  FIFO0  FIFO0
                              REOF   FF     HF     EF     REOF   FF     HF     EF     REOF   FF     HF     EF     REOF   FF     HF     EF


fifo=    0x0010               D31 ------------------------  SEE CAL FIFO DATA READOUT SECTION (BELOW)  ------------------------------- D00
READ

intcntl=  0x0040                                                                       D07 -----  SEE GLAST VME S/W USER'S GUIDE  ---- D00
READ/WRITE

*********************************************************************************************************************************************

/* CAL READOUT FPGA REGISTERS */

cntlreg=  0x0200              D15   D14   D13   D12   D11   D10      D09      D08     D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE                           H     H     H     H     H       H/L      H/L      H      L                   H      H      H      H
FPGA CONTROL REGISTER          -    99uS  BIST  L1T   TREQ  CPU      RDO      RDO     DTC    DTC    CMD    CMD    CNTR   TIMR   REGS  LOGIC
DEFAULT= 0x0000                     L1T   EN    EN    EN    BSY    640/-160   BSY    HFULL  HFULL  CBL    CBL    CLR    CLR    CLR    CLR
                                    TIMR                                    MAX/-MIN  EN     CLR    SEL1   SEL0


cmdreg=  0x0204               D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE
CAL COMMAND REGISTER          ------------------------  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION  ----------------------------------
DEFAULT= 0x0000
SELECT CMD CABLE FIRST!  MONITOR statreg FOR CAL HSK RESPONSE, GET HSK RESULT FROM hskstat.


statreg= 0x0208               D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ                                                                                                         H      H      H      H      H
STATUS REGISTER                -      -      -      -      -      -      -      -      -      -      -    SDATA  SDATA  SDATA   HSK    HSK
DEFAULT= 0x0000                                                                                             RDO   RDO LNG  RDO    PAR    RDO
                                                                                                           TMOUT   BSY    BSY    ERR    BSY
```

```
mskreg=  0x020C               D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE                     H      H      H      H      H      H      H      H      H      H      H      H      H      H      H      H
L1T I/O, ACD VETO ENABLES     L1T    L1T    L1T    L1T    L1T    L1T    ACDL   EXT    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL
EXT, CAL TREQ ENABLES         OUT    OUT    OUT    IN     IN     IN     VETO   TREQ   TREQH  TREQH  TREQH  TREQH  TREQL  TREQL  TREQL  TREQL
H= ENABLE, L= DISABLE         MSKC   MSKB   MSKA   MSKC   MSKB   MSKA   MSK    MSK    MSK3   MSK2   MSK1   MSK0   MSK3   MSK2   MSK1   MSK0
DEFAULT= 0xFC00                                                                    (XCAL3)(XCAL2)(XCAL1)(XCAL0)


tstreg=  0x0210               D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE                                   H      H      H      H      H      H      H      H      H      H      H      H      H      H
L1T INPUT, ACD VETO TEST       -      -     L1T    L1T    L1T    ACDL   CPU    EXT    CAL    CAL    CAL    CAL    CAL    CAL    CAL    CAL
CPU, EXT, CAL TREQ TEST                     IN     IN     IN     VETO   TREQ   TREQ   TREQH  TREQH  TREQH  TREQH  TREQL  TREQL  TREQL  TREQL
H= PULSE ON, L= OFF                         TSTC   TSTB   TSTA   TST    TST    TST    TST    TST    TST    TST    TST    TST    TST    TST
DEFAULT= 0x0000


rngreg= 0x0214                D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE
ACD VETO 1SHOT RANGE          ACDLR7 ACDLR6 ACDLR5 ACDLR4 ACDLR3 ACDLR2 ACDLR1 ACDLR0 CALR7  CALR6  CALR5  CALR4  CALR3  CALR2  CALR1  CALR0
CAL TREQ 1SHOT RANGE          VETO   VETO   VETO   VETO   VETO   VETO   VETO   VETO   TREQ   TREQ   TREQ   TREQ   TREQ   TREQ   TREQ   TREQ
DEFAULT= 0x1E14 (1.5/1uS)


nevents_thresh= 0x0218        D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ/WRITE
NEVENTS THRESHOLD REGISTER     -      -      -      -      -      -      -     NET08  NET07  NET06  NET05  NET04  NET03  NET02  NET01  NET00
DEFAULT= 0x0001


nevents= 0x021C               D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ                                         H      H      H      H      H
NEVENTS REGISTER               -      -     FIFO   FIFO   NEVNT  NEVNT  NEVNT  NEV08  NEV07  NEV06  NEV05  NEV04  NEV03  NEV02  NEV01  NEV00
DEFAULT= 0x0000                             FULL   HFULL  FULL   EMPTY   RDY
                                            TRAP   TRAP                 THRSH


gps_timecap1= 0x0220          D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
GPS TIME CAPTURE              GPS15 GPS14  GPS13  GPS12  GPS11  GPS10  GPS09  GPS08  GPS07  GPS06  GPS05  GPS04  GPS03  GPS02  GPS01  GPS00


gps_timecap2= 0x0224          D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
GPS TIME CAPTURE              GPS31 GPS30  GPS29  GPS28  GPS27  GPS26  GPS25  GPS24  GPS23  GPS22  GPS21  GPS20  GPS19  GPS18  GPS17  GPS16

***********************************************************************************************************************************************

/* CAL READOUT FPGA HOUSEKEEPING RAM */

hskstat=  0x0100              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
CMD HOUSEKEEPING STATUS       ------------------------  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION  ---------------------------------


hskcntr0= 0x0104              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
CMD HOUSEKEEPING COUNTER 0    CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0   CTR0
                              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
WRITE CMD 0x00XX TO RECEIVE COUNTERS 0 THROUGH 39 FROM CAL.  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION.
```

```
hskcntr1= 0x0108              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
CMD HOUSEKEEPING COUNTER 1    CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1   CTR1
                              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
WRITE CMD 0x00XX TO RECEIVE COUNTERS 0 THROUGH 39 FROM CAL.  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION.

hskcntr2= 0x010C              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
CMD HOUSEKEEPING COUNTER 2    CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2   CTR2
                              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
WRITE CMD 0x00XX TO RECEIVE COUNTERS 0 THROUGH 39 FROM CAL.  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION.

hskcntr3= 0x0110              D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
READ
CMD HOUSEKEEPING COUNTER 3    CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3   CTR3
D15    D14    D13    D12    D11    D10    D09    D08    D07    D06    D05    D04    D03    D02    D01    D00
WRITE CMD 0x00XX TO RECEIVE COUNTERS 0 THROUGH 39 FROM CAL.  SEE CAL ICD COMMAND/HOUSEKEEPING DOCUMENTATION.
                                                                        :
hskcntr4=  0x0114                                                       :

hskcntr34= 0x018C                                                CONTINUED AS ABOVE
hskcntr35= 0X0190
hskcntr36= 0X0194                                                       :
hskcntr37= 0X0198                                                       :
hskcntr38= 0X019C                                                       :
hskcntr39= 0X01A0                                                       :
```

****

/* CAL FIFO DATA READOUT */

Send CMD 0x2000 through 0x2003 and set bit "RDO 640/-160" low for normal 160-ADC calorimeter readout. Send CMD 0x2004 and set bit "RDO 640/-160" high for 640-ADC calibration mode readout. 160-ADC readout commences four times with same trigger counter, trigger timer, and STAT/TREQ/VETO capture word values each time, but ADC gains stepped in sequence. Only the last Dead Time Cause/Dead Time word value is valid in the 640-word mode (INVALID if 99Us L1T timer enabled).

```
Word Number        32... data bits ...16       15... data bits ...0

0                        Trigger Counter Word (32-bits)
1                         Trigger Timer Word (32-bits)
2                       STAT/TREQ/VETO Capture (13-bits)                         STAT/TREQ/VETO Capture
3                  X+ Cbl 0 Chan 0 ADC 0     X- Cbl 2 Chan 4 ADC 0               D12: Readout 640 Words (H) or 160 Words (L)
4                     Cbl 0 Chan 1 ADC 0        Cbl 2 Chan 3 ADC 0               D11: Readout Busy Max (H, non-pipelined) or Min (L, pipelined)
5                     Cbl 0 Chan 2 ADC 0        Cbl 2 Chan 2 ADC 0               D10: ACDL VETO
6                     Cbl 0 Chan 3 ADC 0        Cbl 2 Chan 1 ADC 0                D9: CPU TREQ
7                     Cbl 0 Chan 4 ADC 0        Cbl 2 Chan 0 ADC 0                D8: EXT TREQ
8                  Y+ Cbl 1 Chan 4 ADC 0     Y- Cbl 3 Chan 0 ADC 0                D7: CAL TREQH 3 (ignore)
9                     Cbl 1 Chan 3 ADC 0        Cbl 3 Chan 1 ADC 0                D6: CAL TREQH 2 (ignore)
10                    Cbl 1 Chan 2 ADC 0        Cbl 3 Chan 2 ADC 0                D5: CAL TREQH 1 (ignore)
11                    Cbl 1 Chan 1 ADC 0        Cbl 3 Chan 3 ADC 0                D4: CAL TREQH 0 (ignore)
12                    Cbl 1 Chan 0 ADC 0        Cbl 3 Chan 4 ADC 0                D3: CAL TREQL 3
13                 X+ Cbl 0 Chan 0 ADC 1     X- Cbl 2 Chan 4 ADC 1                D2: CAL TREQL 2
14                    Cbl 0 Chan 1 ADC 1        Cbl 2 Chan 3 ADC 1                D1: CAL TREQL 1
15                    Cbl 0 Chan 2 ADC 1        Cbl 2 Chan 2 ADC 1                D0: CAL TREQL 0
16                    Cbl 0 Chan 3 ADC 1        Cbl 2 Chan 1 ADC 1
17                    Cbl 0 Chan 4 ADC 1        Cbl 2 Chan 0 ADC 1
18                 Y+ Cbl 1 Chan 4 ADC 1     Y- Cbl 3 Chan 0 ADC 1
19                    Cbl 1 Chan 3 ADC 1        Cbl 3 Chan 1 ADC 1
20                    Cbl 1 Chan 2 ADC 1        Cbl 3 Chan 2 ADC 1
21                    Cbl 1 Chan 1 ADC 1        Cbl 3 Chan 3 ADC 1
22                    Cbl 1 Chan 0 ADC 1        Cbl 3 Chan 4 ADC 1
23                 X+ Cbl 0 Chan 0 ADC 2     X- Cbl 2 Chan 4 ADC 2
24                    Cbl 0 Chan 1 ADC 2        Cbl 2 Chan 3 ADC 2               Dead Time Cause/Dead Time
25                    Cbl 0 Chan 2 ADC 2        Cbl 2 Chan 2 ADC 2               D21: XCAL Busy
26                    Cbl 0 Chan 3 ADC 2        Cbl 2 Chan 1 ADC 2               D20: Readout L1T Wait
27                    Cbl 0 Chan 4 ADC 2        Cbl 2 Chan 0 ADC 2               D19: CPU Busy
28                 Y+ Cbl 1 Chan 4 ADC 2     Y- Cbl 3 Chan 0 ADC 2               D18: Data FIFO Full Trap
29                    Cbl 1 Chan 3 ADC 2        Cbl 3 Chan 1 ADC 2               D17: Data FIFO Full
30                    Cbl 1 Chan 2 ADC 2        Cbl 3 Chan 2 ADC 2               D16: Data FIFO Half Full Trap
31                    Cbl 1 Chan 1 ADC 2        Cbl 3 Chan 3 ADC 2               D15: Data FIFO Half Full
32                    Cbl 1 Chan 0 ADC 2        Cbl 3 Chan 4 ADC 2               D14: CAL Readout Busy
 .                             .                          .                      D13 - D0: Dead Time Counter (x 50ns)
 .                             .       etcetera           .
 .                             .                          .
 .                             .                          .
73                 X+ Cbl 0 Chan 0 ADC 7     X- Cbl 2 Chan 1 ADC 7
74                    Cbl 0 Chan 1 ADC 7        Cbl 2 Chan 3 ADC 7
75                    Cbl 0 Chan 2 ADC 7        Cbl 2 Chan 0 ADC 7
76                    Cbl 0 Chan 3 ADC 7        Cbl 2 Chan 2 ADC 7
77                    Cbl 0 Chan 4 ADC 7        Cbl 2 Chan 4 ADC 7
78                 Y+ Cbl 1 Chan 4 ADC 7     Y- Cbl 3 Chan 1 ADC 7
79                    Cbl 1 Chan 3 ADC 7        Cbl 3 Chan 3 ADC 7
80                    Cbl 1 Chan 2 ADC 7        Cbl 3 Chan 0 ADC 7
81                    Cbl 1 Chan 1 ADC 7        Cbl 3 Chan 2 ADC 7
82                    Cbl 1 Chan 0 ADC 7        Cbl 3 Chan 4 ADC 7
83                       Dead Time Cause/Dead Time (21-bits)
```