



GLAST Mission Interface Change Notice (ICN)

SPECTRUMASTRO

ICN No.

032

SHEET 1 OF 2

ORIGINATOR: Tim Morse

PHONE: 480-892-8200

DATE: 10-2-03

CHANGE TITLE: LAT Science Data Name Consistency

ORG: Spectrum Astro

DOCUMENT NUMBER

TITLE

VERSION

1196-EI-Y46311-000

LAT-SC ICD

A

REASON FOR CHANGE:

Standardize on the name of the SC Ready and LAT Valid signals in the text and graphics.

PROPOSED CHANGE:

See next page.

INSTRUMENT IMPACT

- Cost
- Schedule

SPACECRAFT IMPACT

- Cost
- Schedule

ORIGINATOR SIGNATURE:

APPROVAL SIGNATURES:

Spectrum Instrument Interface Lead – Tim Morse

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6.4.1.1 LVDS Science Data Interface Timing

The LAT/GBM Input/Output (LGIO) shall receive data from the LAT at a rate up to 66Mbps.

The timing operation of the LAT interface is described below and shown in Figure 6-12 and Table 6-2.

- a. The LGIO shall indicate that it is ready to receive a data “block” by activating the $\overline{\text{LAT_SC_RDY}}^*$ signal on the falling edge of LAT_CLK.
- b. The LAT may start to transmit data any time after the $\overline{\text{LAT_SC_RDY}}^*$ signal is active on the rising edge of the LAT_CLK.
- c. The LAT places data on LAT_DATA lines and activates LAT_VAL* on rising edge of LAT_CLK.
- d. The LGIO latches the data on the falling edge of LAT_CLK when LAT_VAL* is active.
- e. When the LAT needs to pause data flow it shall negate LAT_VAL* on the rising edge of LAT_CLK.
- f. The LGIO shall not latch data when the LAT_VAL* is not asserted during the falling edge of LAT_CLK.
- g. When the LGIO cannot receive a new “block” of data, it shall negate the $\overline{\text{LAT_SC_RDY}}^*$ signal on the falling edge of LAT_CLK.
- h. The LGIO shall continue to receive data from the current “block” after negating the $\overline{\text{LAT_SC_RDY}}^*$.
- i. The LAT shall delay the start of a new block transfer until $\overline{\text{LAT_SC_RDY}}^*$ signal is asserted.

6.4.1.2 LVDS Interface Hardware

Both the LAT and the LGIO shall have $100\ \Omega \pm 10\ \Omega$ terminators on the differential input signals as shown in Figure 6-13.

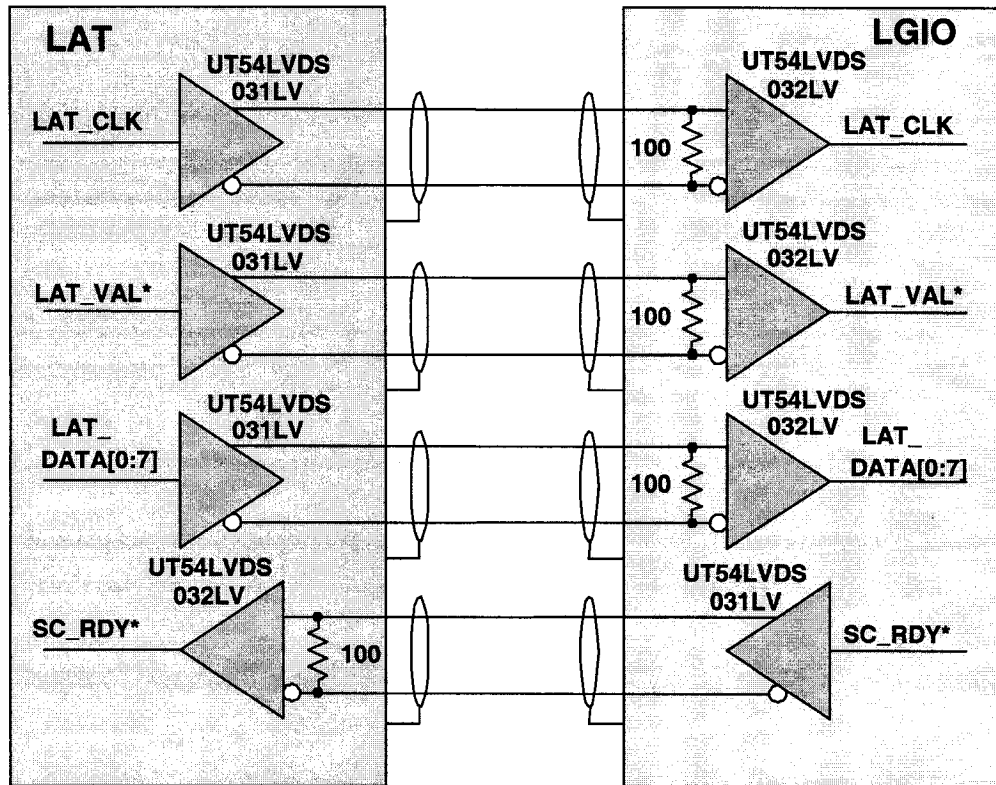
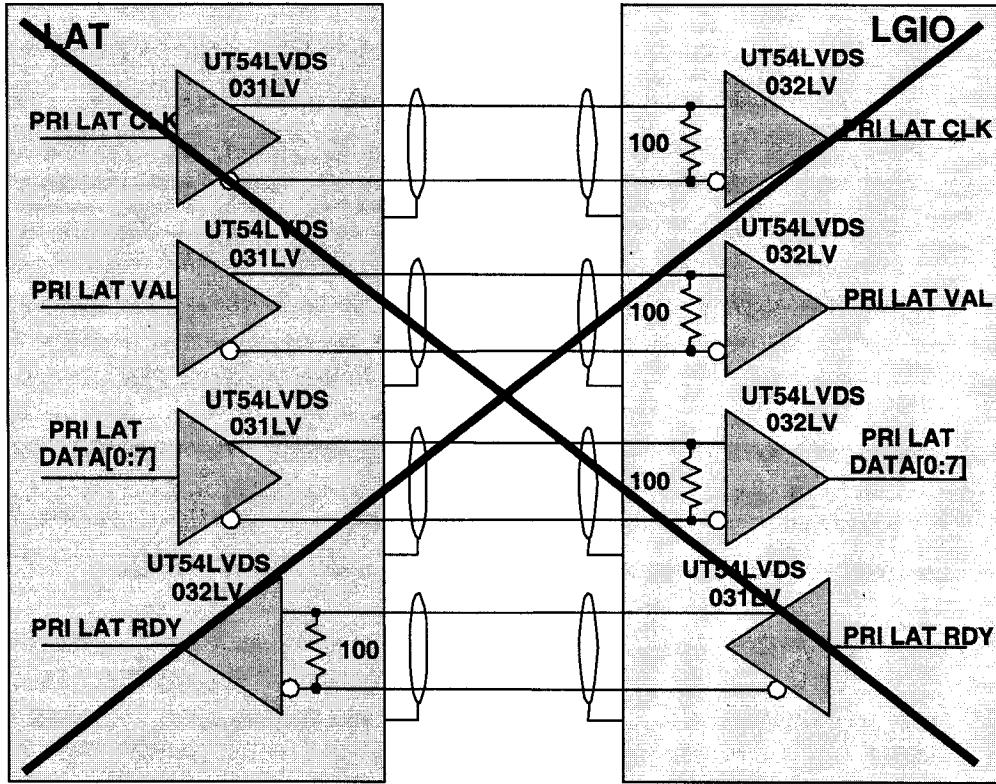


Figure 6-13. LAT/LGIO LVDS Hardware Interface