Special Test Request Form	STR Number 19r1

Part 1 – Test Definition Section

Test Title: AEM/ACD Clock Phase Bit Determination | **Test Requestor**: Rich Baun

Test Purpose and Justification:

Following integration of the ACD to the LAT, the correct setting for the Clock Phase Bit for each AEM/GARC interface must be determined in order to insure robust communications. In addition, a detailed analysis of the timing of the AEM/ACD interface is required to fully characterize the interface.

Test Description:

The test will examine the timing of the data transitions of the ACD relative to the GASU clock. This is done by running a register test while sweeping the frequency with the ACD clocking the data out at the rising edge and with the ACD clocking the data out at the falling edge. Based on where the register test has failures, the time delay can be computed, and the flight setting for the ACD data clocking can be determined.

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GSE Configuration:

EGSE required to provide an external clock to the LAT in place of the 20MHz clock.

LAT Configuration:

Sixteen Towers in the Grid, Flight GASU, Flight PDU, and ACD installed with flight cables. The ACD, PDU, and GASU are powered On and the TEMs, CAL, and TKRs powered Off. EMI shield, ground panel, and Bulkhead Bracket (or equivalent) needs to be installed to support flight cables.

Expected Results/Acceptance Criteria:

Determine and set the Clock Phase Bit for each GARC Mode Register such that no data transport errors occur in all AEM/GARC communications.

Expected Duration: 4 Hrs

Expected Analysis Duration: 1 Hr

Test Procedure:

The description below defines the test. I&T can modify the sequence if necessary for test efficiency.

1) Loop on frequency from 18MHz to 22 MHz in 0.25 MHz increments. For each frequency step, run the script AcdGarcRegRdWr.py documented in paragraph 4.3 item O) of the ACD CPT, ACD-PROC-000270. Use the GARC Mode Register default Clock Phase Bit configuration (clock on negative edge). Record the pass/fail state of the register test for each FREE card.

2) Repeat step 1 with the GARC Mode Register set to clock on the other edge.

3) If no errors have been observed, repeat the first two steps with the frequency loop starting at 18MHz and decreasing by 0.25 MHz increments until the frequency reaches 14 MHz.

Test Scripts:

1) AcdGarcRegRdWr.py.

Part 2 – Impact Assessment Section

Procedure development:

Write in the schemas / steps in work order

Script development and checkout:

Use "off-the-shelf" script, but we need new schemas from online

Impact to schedule:

1 shift.

Risk Assessment:

No significant risk.

Required Resources:

- 3 hrs of online time to make the new schemas
- 1-hr Brian Grist to write the work order
- 1 shift of test conductor/operator/QA to execute test
- 2-hrs of John Canfield to update procedures to reflect as-determined clock phase

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Other Affected Parties:

None.

Part 3: Signature Approval:

Required Authorizations	Printed Name	Signature	Date
Quality	Joe Cullinan	(Signature on file)	12/13/05
I&T	Ken Fouts	(Signature on file)	12/13/05
Program Office	Lowell Klaisner or Dick Horn	(Signature on file)	12/14/05
Systems Engineering	Pat Hascall	(Signature on file)	12/13/05
Affected S/S managers	N/A		
Instrument Scientist	Steve Ritz or Eduardo do Couto e Silva	(Signature on file)	12-13-05
IFCT	Larry Wai	(Signature on file)	12-09-05
DAQ	Gunther Haller	(Signature on file)	12-09-05
DAQ	Mike Huffer		
