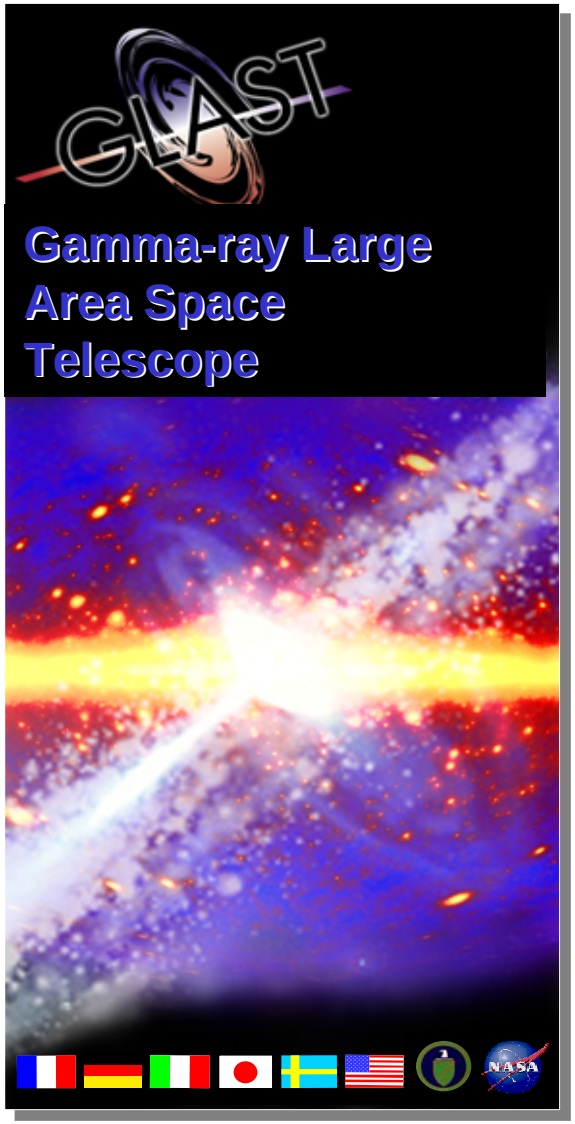

GLAST Large Area Telescope:

Results of LAT Level Test Issues Meeting Held on 10/28

Pat Hascall

Overview

- On October 28, we held a meeting to resolve a few remaining LAT level test issues
- The guests of honor were Mike Huffer and JJ
  - Other attendees were Dick Horn, Neil Johnson, Anders Borgland, Lester Miller, Selim Tuvi, and Ric Claus
- Additionally we discussed the use of test points.
  - The IRD states that “Data collected to verify acceptance or qualification of performance requirements shall be acquired through flight interfaces and not through test point interfaces“.
  - Our interpretation is that the LATTE 4x based testing defined below is not verification of LAT level performance requirements.

Results

- LRS counter testing / verification
  - The LRS counters functionality is sold off at box level and will be demonstrated in test case LAT22x (Science Mode Demo)
  - No LAT level test for CAL or TKR requires LRS counters.
    - For the ACD HLDCAL, we will use the calibrations acquired using LATTE 4x tests.
    - We do need a test that demonstrates CNO detection that uses charge injection and either event data or LRS counters. (part of vetohitmap test in ACD CPT)
- Register test
  - Near term we will use LATTE 4x based test and the GASU register tests (Test case LAT05x).
    - This will be part of the testing done before LAT ships to NRL, and may be repeated at NRL.
    - According to Mike, GASU register tests must be augmented with TEM reg tests and ACD register tests
  - We will consider adding a FSW based register test as a diagnostic later. A potential interim solution is the “poor mans” register test that uses LATC to load 4 or so bit patterns (requires FSW change).

Results (Continued)

- Time tag accuracy
  - The LAT part of this test will be put in the trigger tests.
    - The test is based on triggering the LAT with the 1PPS and examining the event time tags – this will demonstrate time tags at a point in the 1 second cycle.
    - Part of LAT21x
  - The second piece is tests on the test bed that demonstrate time tags across the entire 1 second cycle. Analysis will be used to combine the test results to show that the LAT will meet the time tag accuracy requirements.
- Flow control
  - A LATTE 4x based test (ported from subsystems) will verify that the flow control functionality is working at the LAT level within the data flow portion of the LAT.
    - Run once via LATTE4x at the beginning of phase 2
  - There needs to be a FSW filter that will not respond to events to check the flow control between data flow and FSW. (part of test case LAT21x)

Results (Continued)

- Frequency margin tests
  - This will be the CAL, Tracker and ACD LPTs run at 18 and 22MHz. (TBR)
  - This is a one time test during the engineering checkout of the LAT, after integration of all 3rd layer boxes
- LAT input voltage margin tests
  - The LAT will be tested with input voltage at 27 and 29V.
  - The subsystem LPTs will be performed. (Or a short muon run)
  - Test case LAT03x
- Verification of attitude information from the spacecraft
  - The FQT (or test on the testbed) will verify that the spacecraft geometry is correctly used to determine GRB position by feeding in the simulation of a GRB at a known location.
  - At the LAT level, we only need to demonstrate that the attitude information is correctly transported across the interface (Part of test case LAT23x)
- Parity bit tests
  - Use DAQ LATTE 4 based test that does this function.
  - It will be run one time before shipment to NRL
  - First part of phase 2