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<td>LAT-TD-04319-01</td>
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<tr>
<th>Author(s)</th>
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<tr>
<td>Gunther Haller</td>
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**Document Title**

Limitations and Deviations for CAL FM Test-Stand #8
## CHANGE HISTORY LOG

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<tr>
<th>Revision</th>
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<td>01</td>
<td>16 August 2004</td>
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Limitations and Deviations for CAL FM Test-stand #8

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Limitations and Deviations for CAL FM Test-stand #8

1. **SCOPE**

This document lists

- the environmental limitations and
- the differences of the test-stand shipped compared to the released test-stand drawings

2. **ENVIRONMENTAL CONDITION**

- The test-stand was only tested at room-temperature.

3. **DIFFERENCES TO RELEASE DRAWINGS**

3.1 **Tower Power Supply**

- LAT-DS-02389-01, PWB, complete
- LAT-DS-02390-04, Schematic: Sheet 1 - R1,R2,R11,R12 not loaded; Sheet 2, ZVR4 not loaded. Other sheets: Capacitors added across TRK Power Switch changed from 0.1µF to 1.0µF. Changed D500 to 1N4489. R532 = 402K.
- LAT-DS-02391-04, Material list, complete
- LAT-DS-00995-06, LAT-DS-00996-04, TPS enclosure: Entire unit is electroless nickel plated. No hard anodized was used.
- Added strip kapton tape below TEM to TPS connector
- Assembly number was not marked on chassis

3.2 **Tower Electronics Module**

- LAT-DS-01650-02 - Schematic Diagram, TEM CCA
- LAT-TD-02230-01 - Bill of Materials, TEM CCA
  - For resistors R648, R649, R650, R651 instead of single 50 Ohm value, two 100 Ohm resistors in parallel are used. They loaded with one soldered on top of second resistor.

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Limitations and Deviations for CAL FM Test-stand #8

- LAT-DS-01646-04 - Circuit Card Assembly, TEM DAQ
- LAT-DS-01649-05 - Printed Wire Board, TEM
- LAT-DS-02583-01 - PWB Fab, Loading and Assembly
- LAT-DS-02588-02 - Connector and Cable Assembly, TEM CCA
- LAT-DS-00554-06 - TEM Box Base
  - Part is fully electroless nickel plated, no hard anodize was used
- LAT-DS-00555-06 - TEM Box Lid
  - Part is fully electroless nickel plated, no hard anodize was used
- LAT-DS-01481-04 - Assembly, Tower Electronics Module
  - Assy number not marked on chassis
- LAT-DS-01026-02 - TEM Connector Plate – countersink both sides equal
- LAT-DS-01031-02 - TEM Connector Pin
- LAT-TD-01880-01 - VHDL, LAT TEM GTIC FPGA
- LAT-TD-01881-01 - VHDL, LAT TEM GTIU FPGA
- LAT-DS-03582-01 - Spacer, TEM Connector – dimension 0.72 in overall length

FPGA version numbers:
  - U45 – GTIC – version 1
  - U62 – COMMCTL version 1 (Preprogrammed firmware version 9)

4. **CHANGES FROM TEST-PROCEDURE**

The test-procedure was in the process of official LAT-DOC release while the tests were performed. No changes to the procedure were done between the executing the tests and official release of the procedure.