**ASIC Root Cause Analysis:**

The root cause of this problem was a lack of clear instructions to Grinding and Dicing Service, Inc. (GDSI). GDSI picked die that were either not tested, or were over the edge of the wafer, or both. The text of section 3.3.8.1 of LAT-PS-01321, the wafer grinding and dicing specification is provided here for reference:

> The T2CY wafers have been probed and tested, and known bad die will be ink-marked by the buyer. Only the whole, known-good AB die (GTFE G3) from each reticle shall be picked and packaged in ESD-safe waffle packs in a manner that ensures traceability to the wafer lot and wafer number within that wafer lot. Partial die at the wafer edges shall not be picked.

We did not define edge die in a manner that would preclude the unprobed, whole die (shaded green in Figure 1) from being picked, packaged, and delivered by GDSI. Additionally, we did not specify that whole die which overlap the wafer scribe mark (shaded black in Figure 1) were to not be picked, packaged and delivered.

Figure 1 shows a map of the wafers containing the GTFE die from MOSIS run T2CY. There are three AA die and four AB die per reticle copy. The AA die are GTFEF V3 ASICs which are non-flight, while the AB die are GTFE G3 ASICs which are flight. Note that that the scribe line on the wafer, which denotes the useable area of the wafer, bisects or is very close to several die. These are referred to as edge die. On previous iterations of the ASIC fabrication, edge die demonstrated poor performance or did not work at all, therefore, it was decided that edge die were not to be used. All of the green-shaded or non-blacked-out AB die were tested using a wafer probe station and die that failed this test were ink marked by the probe station. Die that are blacked out in Figure 1 were not tested. The wafer probe leaves minute marks on the bond pads of the ASIC which can be seen clearly at 30X or greater magnification.

As specified in LAT-DS-01321, GDSI performed a Mil-Std-883E, Method 2010.10 condition B inspection on the die after they were diced. This is an automated inspection using a high-magnification, computer-controlled adaptive-optics system that has the Method 2010.10 pass/fail criteria pre-programmed. The system operator used selected die from multiple wafers to teach the system how to recognize good die, then the system automatically inspected each die by comparing it with what it had been taught and the pass/fail criteria. This inspection is performed on the diced wafers and generates a picking map for the die picking equipment. Un-inked AB die that passed this inspection were picked and packaged and shipped to SLAC. It was believed that this inspection was sufficient.
Figure 1. T2CY Wafer Map
**Corrective Action:**
For current production activities, have Teledyne inspect all on-hand ASIC inventory for die missing probe marks and dicing defects that may have been missed by GDSI. Die found to be defective during this inspection shall be returned to SLAC for final disposition.

Future order and delivery:
Revise LAT-PS-01321 to include specific inspection criteria for probed and edge die.

**Deleted:**
- No visual inspection at UCSC prior to shipping the products to SLAC.
- No visual inspection at SLAC when received products from GDSI to ensure that GDSI delivers quality products.
- No visual inspection at SLAC to ensure production quality chips are shipped out to Teledyne.
- No visual inspection at Teledyne to ensure production quality chips are placed in the kit.

**Action Taken**
- Inspect all ASICs for presence of probe marks, and identify them as “good for production” units. The chips without probe marks shall be segregated and returned to SLAC. This requirement is current and on going.
- SLAC to perform visual inspection prior to shipping to Teledyne.