GLAST Large Area Telescope: Planning Meeting
March 10, 2004
AntiCoincidence Detector (ACD)
Subsystem
WBS: 4.1.6

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Outline – Plan for Lehman Review

- Overview
- Progress/status/problems and resolution
- Path to ACD completion
- Outstanding issues, path to resolution
- Risks and mitigation
- Cost and schedule
LAT Anticoincidence Detector

- **TILE SHELL ASSEMBLY**
  - 89 Plastic scintillator tiles
  - Waveshifting fiber light collection (with clear fiber light guides for long runs)
  - Two sets of fibers interleaved for each tile
  - Tiles overlap in one dimension
  - 8 scintillating fiber ribbons cover gaps in other dimension (not shown)
  - Supported on self-standing composite shell
  - Covered by thermal blanket + micrometeoroid shield (not shown)

- **BASE ELECTRONICS ASSEMBLY**
  - 194 photomultiplier tube sensors (2/tile)
  - 12 electronics boards (two sets of 6), each handling up to 18 phototubes. Two High Voltage Bias Supplies on each board.
ACD Work Flow Overview

- Tile Detector Assemblies 04/04
- Shell 04/04 Subassembly
- ASIC 02/04 Development
- High Voltage Bias Supply 06/04
- Photomultiplier tubes 06/04
- Base Frame 04/04 Subassembly
- Thermal Blanket Micrometeoroid Shield 07/04
- Tile Shell Assembly 06/04
- Front End Electronics Card Assembly 06/04
- Electronics Chassis 06/04
- Base Electronics Assembly 06/04
- ACD Integration 07/04
- ACD Performance and Environmental Test 07/04

Completion Dates Shown

Ship 12/04
# Problems and Resolution

<table>
<thead>
<tr>
<th>Problem</th>
<th>Impact</th>
<th>Resolution</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interference found between waveshifting fibers and tile mounting hardware</td>
<td>Mechanical analysts’ and designers’ time redirected, causing schedule delay.</td>
<td>Some re-work of tile manufacture, plus changes in mountings.</td>
<td>Closed.</td>
</tr>
<tr>
<td>Flight-packaged analog ASICs delivered 6 weeks late; digital ASICs 9 weeks late</td>
<td>Delay in start of electronics assembly</td>
<td>ASICs have been delivered; now in screening and qualification</td>
<td>Closed</td>
</tr>
<tr>
<td>Design flaw in digital ASIC allowed turn-on in non-functioning mode.</td>
<td>Turn-on of ACD jeopardized.</td>
<td>Adding 4 resistors to electronics cards bypassed problem.</td>
<td>Closed</td>
</tr>
<tr>
<td>High voltage capacitor failed lifetime tests.</td>
<td>Delay in start of High Voltage Bias Supply assembly</td>
<td>Replacement part identified.</td>
<td>New capacitor in testing.</td>
</tr>
</tbody>
</table>

**AntiCoincidence Detector**

GLAST LAT Project

March 10, 2004
Tile Detector Assemblies (TDA)

- **Status**
  - All drawings complete
  - 58 of 112 (as of 3/8) TDAs delivered
  - Testing continues. All those tested so far meet requirements

- **Plan**
  - All TDAs delivered by end of April, well before needed for assembly.

Individual TDAs after delivery

Flight TDAs in storage
8x8 mapping of TDA shows good uniformity.

Efficiency vs. threshold. Single phototubes meet requirement at 0.3 MIP threshold (as planned). With both phototubes, substantial margin.
Shell Subassembly

• Status
  • Flight unit assembly complete.

• Plan
  • Shell Subassembly being prepared for mechanical qualification testing
Tile Shell Assembly

• Status
  • Flight composite shell complete; tile detectors being finished and tested.
  • Full-scale mock-up is being used for cable routing.

• Plan
  • Following mechanical unit environmental testing, assembly of detectors onto the shell will start.
ASIC Development

• Status
  • Flight-packaged analog ASIC (GAFE) and digital ASIC (GARC) are in screening and qualification.

• Plan
  • ASICS will begin to be mounted on the electronics cards when screening is completed on March 31.
FRont End Electronics Cards (FREE)

• Status
  • Flight FREE cards manufactured.
  • All parts except ASICs are being installed. (provide assy status at later date)

• Plan
  • ASICs will begin being mounted on the electronics cards when screening is completed on March 31.
High Voltage Bias Supply (HVBS)

- **Status**
  - HVBS boards are complete and in testing; most parts to populate boards are ready.

- **Plan**
  - Assemble HVBS as soon as the new capacitor is qualified.
Photomultiplier Tubes

• Status
  • Flight tubes were purchased and tested some time ago.
  • Assembly of flight mountings and resistor divider networks is starting.

• Plan
  • New assemblies are nearly in production
Electronics Chassis

• Status
  • Completed environmental testing of Engineering Model chassis

• Plan
  • Waiting for phototubes, HVBS, and FREE cards.
Base Frame Subassembly

- **Status**
  - Flight unit complete

- **Plan**
  - Mechanical assembly ready for mechanical qualification testing
Micrometeoroid Shield (MMS)

• **Status**
  • Design is complete. Materials have been purchased.

• **Plan**
  • Fabrication will start soon.
Drawing Status/Plan

105 TOTAL DRAWINGS
50 Released, in CM system
35 Complete, in signoff
20 in progress

Plan for completion – work, work, work
Fabrication, Assembly and Testing status

Number needed in parenthesis

Clear fiber cables (130)

Detector assemblies - TDA - (4 basic types, 89 needed total)

Fiber ribbon detectors (8)

Detector Flexures (366+20 spares)

Base Electronics Assembly (BEA) From next page

Composite Shell Assembly (1)

STATUS KEY

- Prototyped
- In Fabrication or Ordered
- Received
- In assembly
- Assembled
- Tested

Clear fiber cables (130):
- Prototyped: 6
- In Fabrication or Ordered: 130

Detector assemblies - TDA - (4 basic types, 89 needed total):
- Received: 6
- Assembled: 58
- Tested: 58

Fiber ribbon detectors (8):
- Assembled: 8

Detector Flexures (366+20 spares):
- Assembled: 360

Base Electronics Assembly (BEA) From next page:
- Received: 1

Composite Shell Assembly (1):
- Assembled: 1
Fabrication, Assembly and Testing status

Base Electronics Assembly (1)

Electronics Chassis (8) (4 double + 4 single)

Base Frame Assembly (1)

Photomultiplier Tube rails (8 + 2 spares)

Power distribution board (8+2 spares)

Chassis and connector frames (8)

Connectors
## Fabrication, Assembly and Testing Status

<table>
<thead>
<tr>
<th>Electronic Chassis Subassembly Item</th>
<th>Needed</th>
<th>Proto</th>
<th>Assembled</th>
<th>Tested</th>
<th>Ready for higher assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Photomultiplier Tube Assemblies</strong></td>
<td>194 + 46</td>
<td>Yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photomultiplier Tube (PMT)</td>
<td>194 + 46</td>
<td>Yes</td>
<td>240</td>
<td>240</td>
<td>230</td>
</tr>
<tr>
<td>Photomultiplier Tube housings</td>
<td>194 + 46</td>
<td>Yes</td>
<td>240</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photomultiplier Tube resistor networks</td>
<td>194 + 46</td>
<td>Yes</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Front End Electronics (FREE) ‘right hand’ boards</td>
<td>4 + 2 spares</td>
<td>Yes</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Front End Electronics (FREE) ‘left hand’ boards</td>
<td>8 + 2 spares</td>
<td>Yes</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>GLAST ACD Front End chip – GAFE</td>
<td>216 needed, 650 ordered</td>
<td>Yes</td>
<td>800</td>
<td>800</td>
<td>30</td>
</tr>
<tr>
<td>GLAST ACD Readout Controller chip – GARC</td>
<td>12 needed, 125 ordered</td>
<td>Yes</td>
<td>800</td>
<td>40</td>
<td>0</td>
</tr>
<tr>
<td>Digital to Analog Converter - DAC MAX 5121</td>
<td>24 + spares</td>
<td>Yes</td>
<td>36</td>
<td>36</td>
<td>36</td>
</tr>
<tr>
<td>Analog to Digital Converter – ADC MAX 145</td>
<td>216 + spares</td>
<td>Yes</td>
<td>300</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>High Voltage Bias Supplies (HVBS) boards (24 + 6 spares)</td>
<td>24 + 6 spares</td>
<td>Yes</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>High Voltage Capacitors</td>
<td>218 + 52</td>
<td>Yes</td>
<td>218**</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Capacitors failed life testing and are being replaced**
## RISK FOCUS

<table>
<thead>
<tr>
<th>Rank, Title, Criticality</th>
<th>Risk Statement</th>
<th>Approach &amp; Plan</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. EEE Part Failure</td>
<td>If: If a EEE part fails Then: due to the high volume of components, a significant cost and schedule impact will occur.</td>
<td>Mitigate: Order, test, screen, and qualify parts early.</td>
<td>Resolved several issues with high voltage capacitor life testing this month. Two capacitors experienced anomalies during life testing. One can be used for flight, the other is being replaced with a new part. New parts on order and due to be received on March 24.</td>
</tr>
<tr>
<td>2. Schedule / Milestone slips</td>
<td>If: Technical problems can not be rapidly resolved Then: A schedule slip will occur</td>
<td>Mitigate: Identify potential problems early and develop comprehensive plans to solve the problem. Optimize production flow in order to minimize schedule delays. Provide the required level of staffing to complete the task</td>
<td>The digital ASIC was delivered 9 weeks late. This part is on the first critical path for the ACD. Schedule workarounds have pulled in 6 of the nine weeks, however 3 weeks of schedule could not be recovered.</td>
</tr>
<tr>
<td>Rank, Title, Criticality</td>
<td>Risk Statement</td>
<td>Approach &amp; Plan</td>
<td>Status</td>
</tr>
<tr>
<td>-------------------------</td>
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</tr>
</tbody>
</table>
| 3. Aggressive scheduling of E.M. tests, fabrication and I&T due to schedule and cost pressure | If: Any unexpected problems with E.M. or flight subsystem during performance testing, qualification, or I&T. Then: there is little reserve to handle the additional work and schedule delay. | Mitigate
Received additional schedule during LAT rebaseline.
Watch
Careful consideration leads us to believe risks are very minor. Risk for ACD because of volume of our parts and low remaining contingency. | Quickly resolved several issues this month. Performing schedule workarounds to maximize schedule float to our required need date. Currently have 9 weeks of schedule margin. |

| 4. Electrical Interface problem between the ACD and LAT | If: there is an electrical interface problem between the ACD and the LAT. Then: a cost and schedule impact will occur. | Mitigate
Test interface in a flight like condition and as early as possible. Re-test interface whenever a change is made. | ACD Electronics team performed tests using LAT provided electrical cables this month. ACD Team will travel to Stanford Linear Accelerator Center the week of March 22 to support test of LAT/ACD interface. |
Cost and Schedule Here
Format?
Critical Path Analysis
Interdependencies

1. Delivery of FREE Boards and ASICs to Electronics for test bed. – FREE boards delivered; GAFEs and GARCs in screening
2. EGSE/G3 – Ongoing development with I&T and Electronics groups.
   - Valuable visit by Mike Huffer, Ric Claus, Jim Panetta
   - ACD electronics group will visit SLAC March 22, bringing an electronics chassis (4 phototubes, 1 FREE card, 1 HVBS) to help commission G3. At completion, one G3 will be sent to GSFC.
   - Additional G3s needed. Agreed on total of four. Would 5 be possible?
3. Grid to Base Frame match drilling – Outline drawing and available date for work? April, but still working schedule conflicts.
4. Delivery of ACD Calibration Unit or subset to LAT I&T – working details for a late March delivery. The same electronics chassis used for G3 commissioning will be used for the calibration unit.
5. ASICs – all now delivered and in screening.
6. Test Cables – Still working some open questions with Dave Nelson.
7. ICD – Rich Bielawski is helping track a set of needed changes.
Open Design Issues - update

- OPEN: Outline drawing that defines some interfaces with LAT is still not complete (blanket attachment, grounding, cable tie-downs, optical survey mounts). Action Plan: Work with LAT mechanical design team to resolve open issues. Status: Mechanicals are iterating 3D models.

- OPEN: Need updated interface loads following Grid design changes. Action Plan: Review ACD analysis when updated loads are received. ACD will not delay fabrication of mechanical components due to this open issue (slight risk in doing so). Status: Received new loads from Goddard (GLAST), but waiting for official word from LAT.
Issue - Photomultiplier Tube (PMT) Anomaly

- We have now lost 4 phototubes during cold cycles of thermal vacuum testing. None of these were flight tubes, but they were mechanically identical. One in the recent batch had passed a previous TV test. Clearly we have a design problem.
- More detailed analysis than done originally shows higher stresses due to magnetic shielding and uralane bonding material.
- New design, moving magnetic shielding to outside of housing and bonding with RTV, is being qualified.
Issue – GARC Design Problem

• Testing at both Goddard and SLAC has shown that the GARC can sometimes turn on in a permanent reset state.
• Investigating a possible fix to be implemented on the FREE card.
• MRB was held yesterday
Issue – High Voltage Capacitor Problem

- Two high voltage capacitors, one for the HVBS and one for the phototube resistor network, failed lifetime testing.
  - One part was determined to be acceptable
  - The second part had a process problem. A replacement has been found. Screened parts are scheduled for delivery in two weeks.
Concerns

• The biggest concern is that this string of parts problems is consuming manpower for investigations and threatening the schedule.