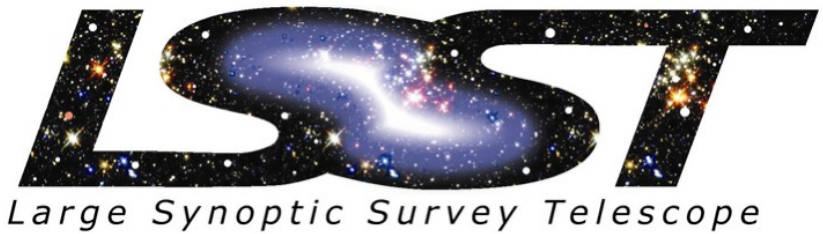
LSST Camera Electronics Overview

September 16, 2008



R. Van Berg for the LSST Electronics Team

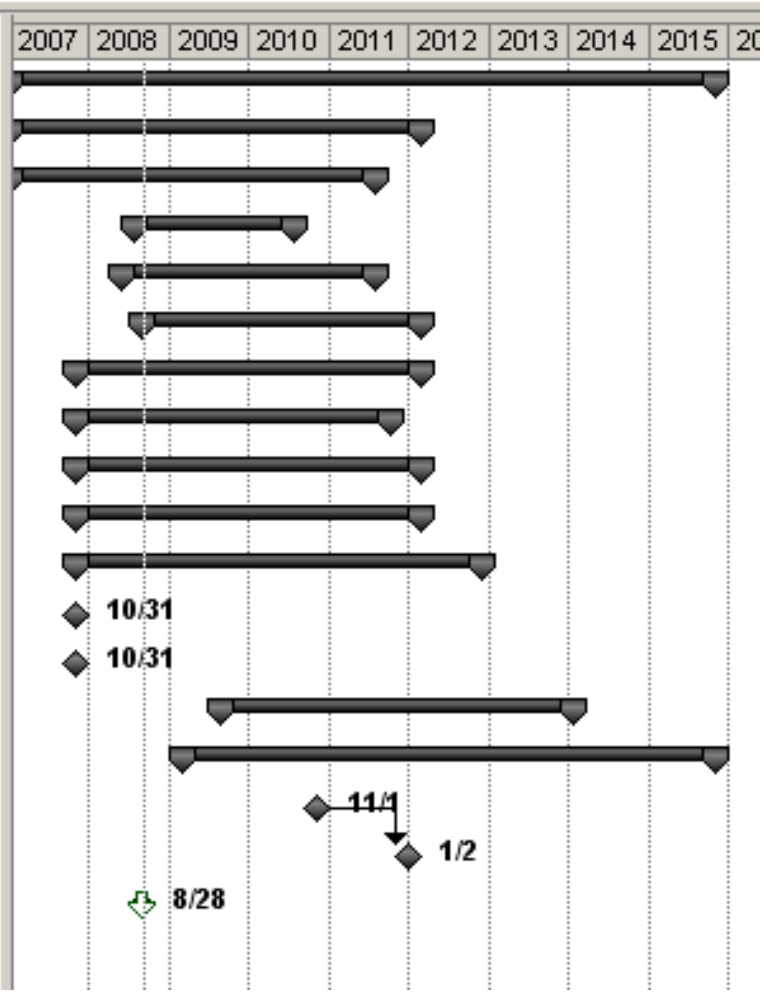
Penn

Outline

- Current plan and schedule for delivery to the Integration and Test phase
- Key technical milestones
- Key technical development activities
- Test requirements/equipment at each phase
- Task interdependencies with other subsystems
- Electronics system self-protection plans and features

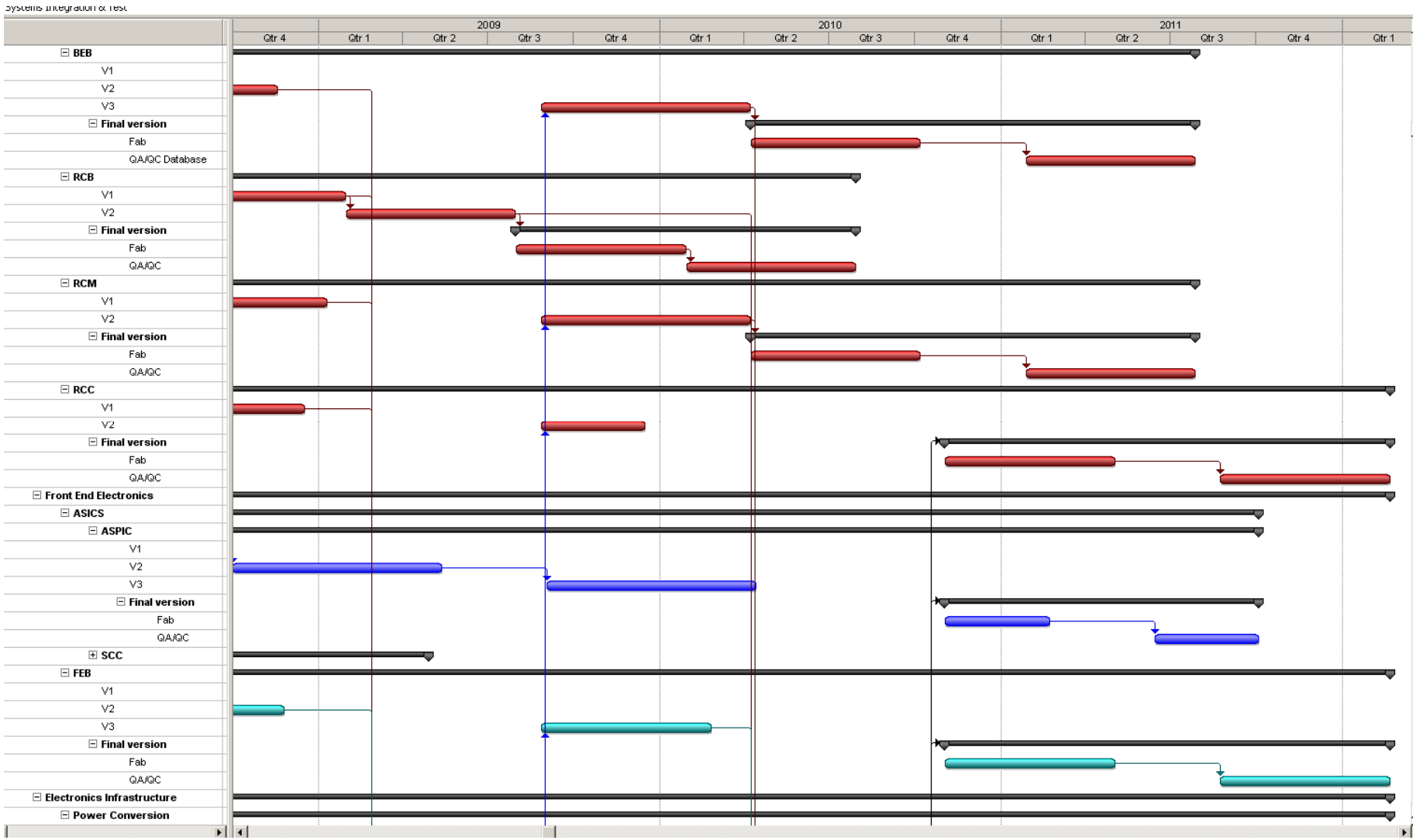
Current plan and schedule for delivery to I&T

WBS	Task Name
3.5.8	**Camera Electronics**
3.5.8.1	**Back End Electronics**
3.5.8.1.1	**BEB**
3.5.8.1.2	**RCB**
3.5.8.1.3	**RCM**
3.5.8.1.4	**RCC**
3.5.8.2	**Front End Electronics**
3.5.8.2.1	**ASICS**
3.5.8.2.2	**FEB**
3.5.8.3	**Electronics Infrastructure**
3.5.8.4	**Controllers & Interface**
3.5.8.5	Electronics Systems Engineering
3.5.8.6	Camera electronics project managment
3.5.8.7	**Corner Raft Electronics**
3.5.8.8	**Systems Integration & Test**
4	Construction start milestone FY'11
5	Construction start controllers
6	Database



Work in progress……

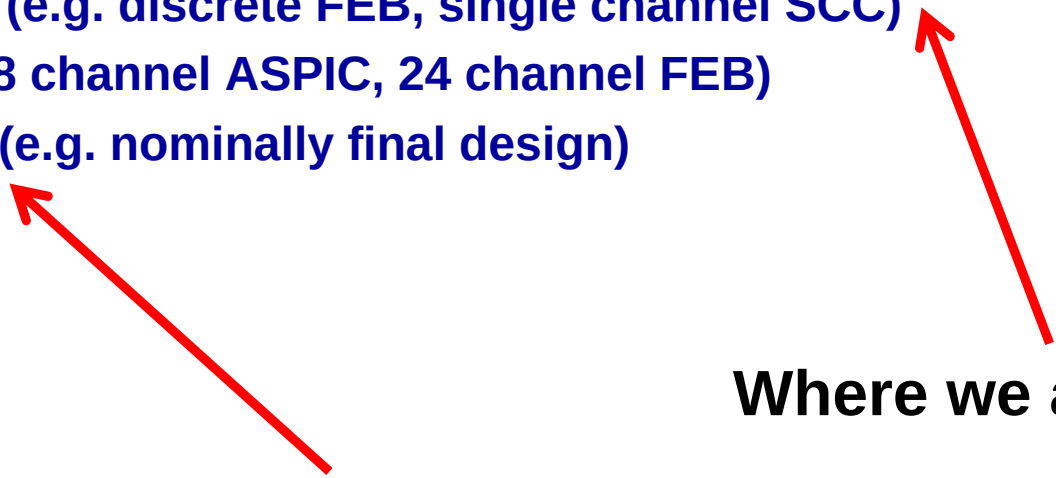
Current plan and schedule for delivery to I&T



Still in progress….

Schedule Cheat Sheet

- Three “phases” of development
  - Early prototype (e.g. discrete FEB, single channel SCC)
  - Prototype (e.g. 8 channel ASPIC, 24 channel FEB)
  - Pre-production (e.g. nominally final design)



Where we are now

Where we need to be end of 2010

CCD Related Milestones:

Proto or Preprod FEBs (1/3 raft) to BNL March (?) 2010
Production FEBs to BNL end of October 2011
Last FEB/BEB to BNL by March 2013

Key technical milestones

- ASIC development:
  - ASPIC – noise, power, crosstalk
  - SCC – power, clock drive
- Front End Board
  - Crosstalk, thermal management, mechanical interfaces
- Back End Board
  - Power, density (e.g. connectors)
- Back End Controller
  - Power, density, high speed I/O
- Infrastructure
  - Power, cabling, cooling, space/mechanics in UT
- Controllers
  - TCM, Fiber interface, other controllers…
- Corner Rafts
  - Guider choice, space, space, space
- Integration
  - Real CCD readout at real LSST rates

Key technical development activities

- **ASIC development –**
  - **ASPIC**
    - Strong IN2P3 Group (LAL Orsay and LPHNE Paris) with some collaboration from Harvard and Penn
    - First version satisfies crosstalk requirement already, not quite on noise (understood)
    - Second version in design – review Oct. 6-8, Boston
  - **SCC**
    - Strong ORNL/UT group
    - First version (single channel of clock and bias) tests ok
    - Second version (full specification) in design – intend to submit in Dec. 08
- **Board development –**
  - **FEB – BEB version 1**
    - Discrete, non-compact 2 channel design demonstrated digitization performance (microVolts) at the level required for LSST
  - **FEB – BEB version 2**
    - Utilize prototype ASPIC / SCC devices, 8 channels (one CCD) – end of this year
  - **FEB – BEB version 3**
    - To use version 2 ASPIC and SCC, full density (24 channels) raft prototypes

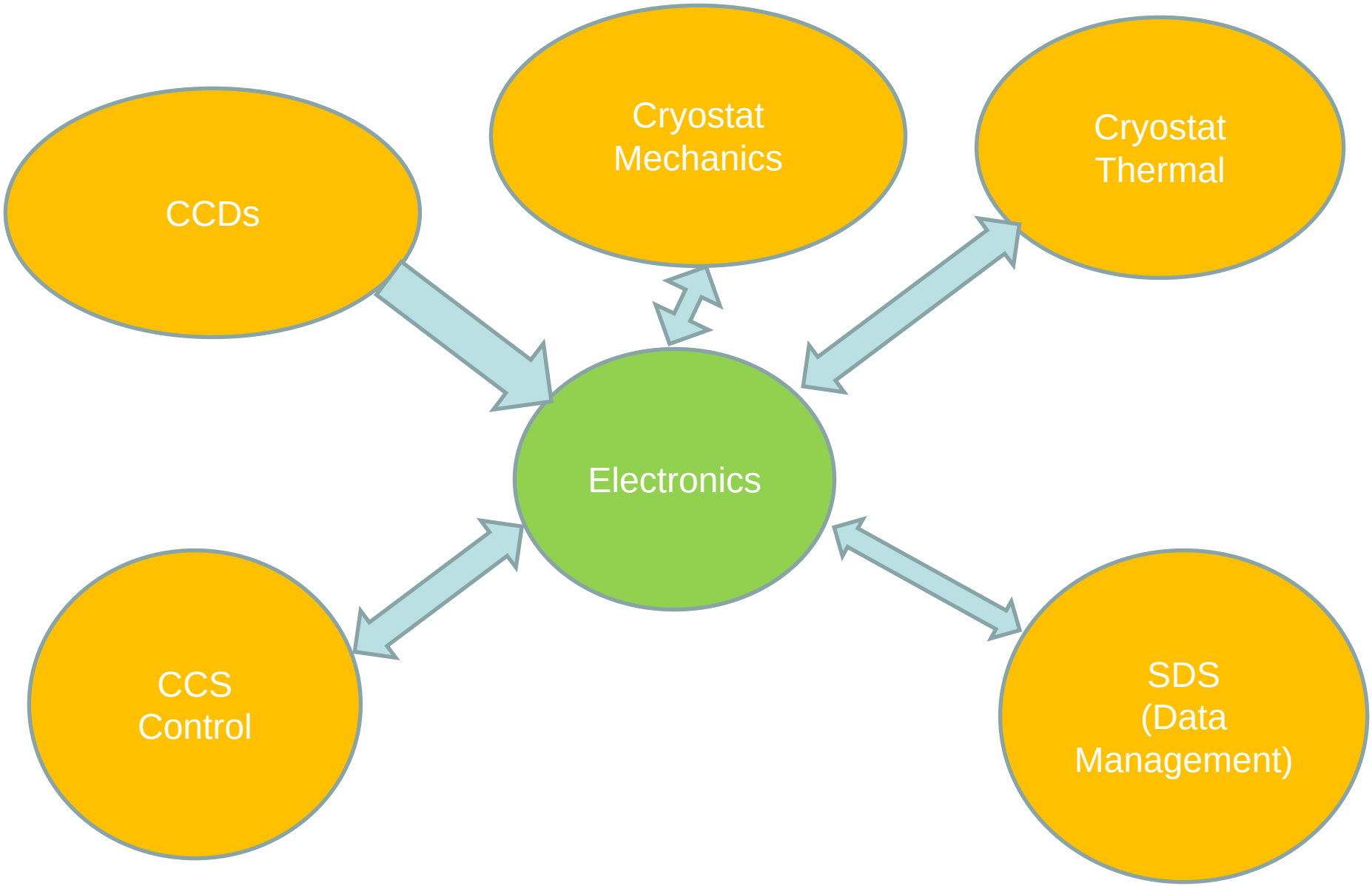
Key technical development activities - II

- **Cabling –**
  - **Inside Cryostat**
    - Kapton CCD→FEB, capacitance, flexibility, connectors
    - Kapton FEB→BEB, flexibility, space
    - “Standard” cable RCM→Flange, routing, space, performance
  - **Outside Cryostat (mostly in Utility Trunk)**
    - Harness design, routing, maintenance
- **Power –**
  - **Conditioning at entry to UT**
  - **AC→DC conversion**
    - Space, noise, reliability, repairability
  - **DC→DC conversion**
    - Space, noise, reliability, repairability

Test requirements/equipment at each phase

- **Early Prototype Phase –**
  - **Point test tools and equipment not yet integrated with CCS or BNL CCD test tools or much of anything else – standard lab equipment**
- **Prototype Phase –**
  - **Incorporate CCS tools as they become available (especially the SDS for data output) – lab equipment plus LSST specific test objects (e.g. CCD simulators) plus real CCD signals.**
- **Pre-Production Phase –**
  - **Full suite of CCS tools (control / monitor plus data flow)**
  - **Full raft / tower mechanical and cooling structures working with raft level CCD metrology and optical test**

Task interdependencies with other subsystems



Task interdependencies with other subsystems

- **Electronics is driven by CCD (and science) requirements**
  - **Noise**
  - **Cross talk**
  - **Stray capacitance**
  - **Speed**
  - **CCD clock and bias specifications**
  - **Cleanliness (e.g. no outgassing of black gook)**

- **Electronics has to be compatible with:**
  - **Data Management -- high speed data output**
  - **Camera Control System – control registers, programming model**
  - **Cryostat mechanics – space, cabling, assembly and repair seq.**
  - **Cryostat thermal – magnitude of heat load, uniformity of load, heat flow**

Electronics system self-protection plans and features

- **Obvious dangers are:**
  - **Overvoltage – regulators to have clamps or OVP**
  - **Overcurrent – regulators to be current limited**
  - **Overheating – loss of cooling needs to cut power to electronics – this is a danger to the camera not really to the electronics (electronics fine at >100C) – an example of a cross task boundary problem**
  -
- **What are the non-obvious dangers we need to protect against?**