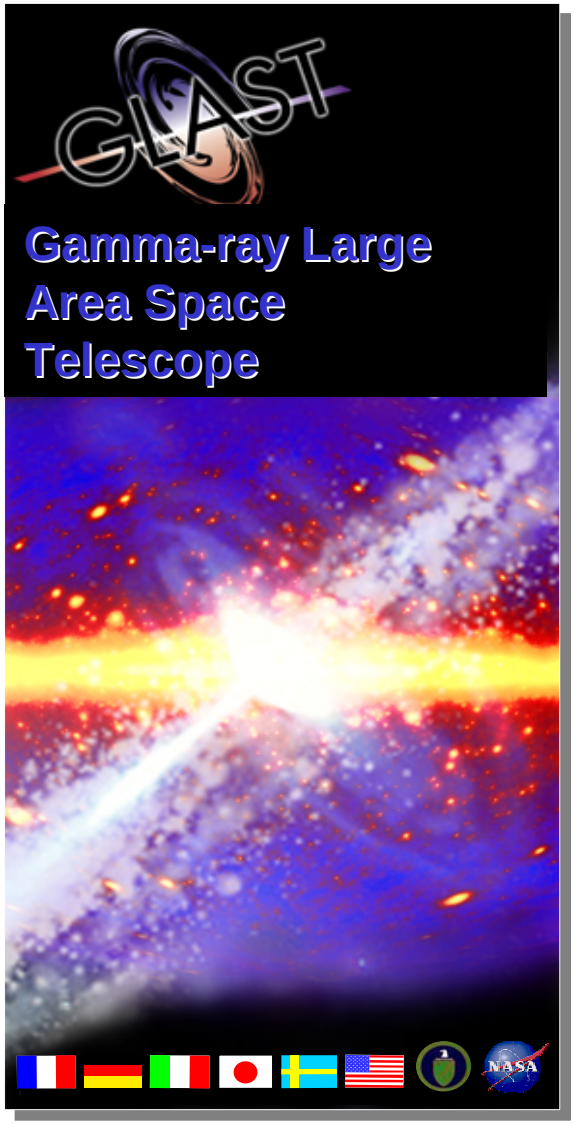

GLAST Large Area Telescope:

Electronics, Data Acquisition & Flight Software W.B.S 4.1.7

Monthly Status 01-05-05

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Test-Stand Summary

Client	Shipped	Assemble/Test	Total
Calorimeter (conformal)	14	0	14
Calorimeter	5	0	5
Tracker (conformal)	2	0	2
Tracker	9	0	9
ACD	4	0	4
I & T* (next slide)	5	0	5
DAQ/FSW	12	0	12
Electronics Support	11	0	11
Total	62	3	62

- **ACD test-stands:**
  - **Last month it was reported that monitoring in one GASU broke**
    - **Received 3/1/05 being fixed, found that shipping container is too small and GASU is vibration tested during shipping, getting bigger container**

ASIC

- All GTCC1, GCCC1 TEM ASIC's screened
  - Qualification testing at GSFC:
    - The parts have passed all of the tests to date.
    - The GTCC and GCCC began the 1000 hr life cycle test on Dec. 15th and completed the 168 hr room temperature test on Dec. 22nd. This test will be complete on Jan. 26th and will then require 3-temperature testing.
    - The other two legs of the qualification testing, HAST and Temperature Cycling, are waiting for the chambers to be available.

- GLTC ASIC's (for GASU)
  - Found problem with GLTC tester board test-socket
    - GLTC3 pins a bit longer than GLTC2 pins, sockets won't work
    - Ordered new sockets, changed layout of test-board, fabricated new test-boards
    - Loaded boards expected 2nd week of January
  - Test software ready
  - Need to test/burn-in/test about 80 devices by 2nd week of February

ACTEL

- UMC line FPGA's
- Programmed, lead-formed 4 sets (one set is one 32 and one 72 series FPGA)
- 3 sets were put on TEM flight boards at assembler
  - Flight TEM passed function/performance tests over temperature
- GSFC DPA'ed several devices
  - Issue with 72-series in regards to bonding to pads
  - Several meetings with SLAC/GSFC/ACTEL took place
  - GSFC got additional 72 from ACTEL
  - ACTEL destructively pulled bonding wires on several additional FPGA's (at Kyocera)
  - Bottom-line is that LAT can use the lot as long as they are not used in single-string system (all LAT elex is redundant)

TEM/TPS Schedule Qual, TWR-A, TWR-B

– TPS & TEM complete with SMT, QA	done
– MECH ASSY TEM and TPS HEATSINK, thru hole, QA	done
– TEM and TPS SPEA	done
– TEM and TPS install cable assys, aqueous clean	done
– TEM and TPS staking, QA	done
– TEM AND TPS available to SLAC engineers to test (passed)	done
– TEM & TPS Conformal Coat, QA	done
– Assemble of TEM & TPS in respective enclosures	1/5/05
– Assemble of TEM to TPS	1/6/05
– Available to SLAC personnel for test	1/7/05
– Vibration test, followed by function/perf test	1/8/05
– Thermal cycle, test, QA	1/11/05
– Review/ship to SLAC	1/16/05
– Receive, test, TV test, test	1/18/05
– EMI test	1/24/05
– Deliver to I&T	2/1/05

- TV chamber being installed in Building 33, needs to be certified by 1/16/05
- EMI contract being placed (RFP responses were received)

- Flight production assembly released 1/5/05
- Start programming of 8 additional sets of FPGA's: 1/10/05
- Flight production schedule: waiting for GT's schedule

GASU & GASU-PS & PDU

- Internal harness for GASU, PDU, SIU
  - Harness using GLENAIR connectors: in fabrication
  - Harnesses not using GLENAIR connectors: To be awarded on 1/7/05
- PDU
  - Enclosure fabricated, due at SLAC 2nd week of January
  - PDU flight boards fabricated
    - failed coupon testing, turned out to be that coupon needed to be modified to reflect board design (so boards would have been ok)
    - However refabricated boards anyways, due 1/7/05
  - Old Issue: OMNIREL linear-regulator. Recalled lot which was received by SLAC. (Tantalum cap used has end-termination with pure Sn as opposed to Sn/Pb. Can't use in space.) New delivery in Feb 05.
- GASU
  - Enclosure in fabrication
  - PCB received (GASU DAQ as well as GASU Power-supply boards)
  - Issue is bug found in trigger algorithm (FPGA VHDL) on test-bed using FES. Logic corrected, needs to be tested
- Testers
  - PDU tester is assembled, code still in progress
  - GASU tester being designed/assembled
  - Details of TV testing to be discussed (can't penetrate TV chamber with all signals)
  - EMI testing order to be created

SIU

- SIU
  - Enclosure in fabrication
  - Flight PWB LCB, CPS, Back-plane in fabrication
  - SIB board in sign-off, then to be fabricated
  - Parts: Issue with PCI ERNI Connector
    - GSFC did DPA on the 6 types of connectors required (flight lots were received months ago)
    - Potential issue is Sn (whiskers). Many connector manufactures removed lead due to environmental issues, but not good for space
    - Turns out that all ERNI connectors fabricated after about 1st quarter of 04 are pure tin (no good for us)
    - Analysis showed that 4 types of connectors are ok, 2 types were not (have later date-code)
    - Yesterday we were able to find some old lot connectors to replace the 2 lots above -> so we are ok
  - SOW for assembly of boards written and released
    - Process is assembly of boards at vendor
    - Testing and crate integration at SLAC
  - Testers and documentation for board and crate tests to be done

Misc

- **LAT Harness**
  - **To be awarded this week (this includes most of the cables, there is a balance of cables needed later which will be on a separate req)**
- **RAD750**
  - **Need to resolve heat-sink issue, will have to send boards back to BAE for rework**

Technical Baseline: DAQ Flight Drawing Release

Group	Total	In Config Control	To Go	In Sign off	Notes
TEM/TPS	48	48	0		
PDU	34	34	0		
GASU	69	56	13		13 to close with FPGA docs
EPU/SIU	59	56	3		3 to close with FPGA docs
Harness	35	32	3	3	
Brackets/hardware	35	29	6	4	
Heater Control Box	21	1	20		

Courtesy of P. Hascall

FSW December Activities

- Charge Injection Calibration (LCI)
  - Work has begun on CAL charge injection code.
- Inter-task Communications System (ITC, LCS, CTS)
  - ITC development continues
- Housekeeping (LHK)
  - Minor bug fixes
  - Performance measurements were made: each Housekeeping collection cycle takes < 500 µsecs, so at 20Hz this is 10msecs, or 1% of the CPU.
- Front End Simulator (FES)
  - Testing of all FES boards is complete
  - File management utilities improved
    - Now have centralized ability to search and create directories on FES PCs, as well as move and copy files
  - Used FES system to evaluate behavior of the GEM
  - Bugs and minor inconsistencies in FES ACD firmware fixed
  - Work has begun to synch FES data with simulated attitude and time-tone message

FSW December Activities (2)

- **Primary Boot Code (PBC)**
  - Implementation of multiple boot code image selection underway
- **File and Memory Management (LFS, FILE, MEM)**
  - File management functionality needed to support demonstration is complete
    - This development effort supports full progress on the 12 (of 14 total) requirements in the early January demo.
  - Post-boot memory management telecommand handlers complete
- **Telecommand and Telemetry Database**
  - Minor adjustments to FSW command and telemetry formats to compensate for bugs in AstroRT
- **LAT Instrument Manager (LIM)/Mode Controller**
  - J. Fisher, M. DeKlotz investigating Spacecraft hardware states and their possible implications for mode control

FSW December Activities (3)

- LAT Diagnostics Framework (LDF)
  - Work in progress
- Instrument Physics (LPA)
  - LAT Data Format (LDF) chosen as the basic representation of event data
  - Currently designing and implementing data compression scheme
- Attitude/Time Processing (LSM)
  - Time processing implementation underway
    - Handling both the internal 20 MHz system clock and time-tone messages over 1553
  - NRL has been working with test attitude data to verify mathematical accuracy of the transformation process
    - Now turning to real-time attitude data
  - Also working on code to generate time and attitude data on the Testbed for testing

FSW Test Status December

- Development of test scripts and test procedures ongoing:
  - Telecommand and telemetry processing test scripts (Test 2a)
  - File and memory management test procedures (Test 2b)
  - FSW and LAT initialization test procedures (Test 9a)
    - SIU Secondary Boot procedures and scripts complete
  - SC <-> LAT discrete signal test procedures (Test 5)
  - Infrastructure for testing of Instrument Physics FSW
- Formal FSW integration plan under development

FSW December Issues

- ITC development is still ongoing
- Understanding Mode Control Requirements
  - Currently reviewing specifications from Spectrum Astro to understand how FSW mode control system must take Spacecraft states into account
- Usage of SCP as FSW test tool must be evaluated

ISIS – Issues resolved since 12/15

#	Description of problem	Due date	Done?
1	JL-2, pin 2 not connected	12-16-04	✓
2	Resolve PCI master abort	12-17-04	✓
3	Upload ISIS FSW build*	1-5-05	
4	Test script: SC Commands	12-17-04	✓
5	Test script: Routing of commands	12-17-04	✓
6	Test script: Ancillary, Attitude and Time Tone Commands	12-16-04	✓
7	Test script: Boot Process	12-17-04	✓
8	Test script: Reset Signal	12-17-04	✓
9	LAT-DS-05398 (Acceptance Test)**	1-6-05	
10	LAT-DS-03541 (Safe Connection)	12-16-04	✓
11	LAT-DS-05297 (Grounding diagram)	12-17-04	✓

* Closure depends on #2 (resolution of PCI master abort)

** Closure depends on #4 – #8 (test script completion)

(SLAC had a two week shutdown: 12/18/04 – 1/2/05)

Test Procedure is available for comment until 2 PM (PST), 1-5-05:

http://www-glast.slac.stanford.edu/Elec_DAQ/ELX_test/content/isis_documentation.htm

Courtesy of J. Thayer

ISIS Summary

- On schedule to ship ISIS early in the 2nd week of January
- The following items were completed on the date given:
  - ✓ Safe Connection Procedure - December 15
  - ✓ Test scripts - December 17
  - ✓ Integrate missing test scripts into Acceptance Test Procedure (LAT-TD-05398) – January 4
  - – Integrate comments into Acceptance Test Procedure - January 6
    - – Comments due by 2 PM (PST), Wednesday, January 5, 2005

MILESTONES

- Acceptance Testing
  - ✓ Run Safe Connection Procedure - December 16
  - – Run Acceptance Test Procedure - January 7
- Post Acceptance Test Review (PATR)
  - – Confirm tests successfully completed (or specify what is required for completion)
- Delivery (ASAP after completion of acceptance tests) – 2nd week of January
  - – After resolution of any existing issues
  - – ISIS shipped, accompanied by team from SLAC; training provided
  - – Installed and verified with a subset of Acceptance Test
  - – Settle on details after Acceptance Tests are complete

Courtesy of J. Thayer

Schedule/Budget

- Total budget: $22,238
- Work Scheduled up to date: $21,007
- Work Performed: $18,469
- Actuals: $21,868
- Schedule Variance $-2,539k (-14%)
  - Qual/Flight work should have been started, reflects current status
- Cost Variance: $-3,400k (-18%)
  - 4.1.7.4 Dataflow $-1,178k
    - ACD Tem EM $-131k
    - ACD TEM FU $-133k
    - LCB FU $-298k
    - GLT FU $-409k
    - Testbed $-509k
    - CPU $+300k (not all boards delivered yet)
  - 4.1.7.5 SIU $-151k
  - 4.1.7.6 Power $-393k
  - 4.1.7.8 Harness $-107k
  - 4.1.7.A EGSE $-1,383k
  - 4.1.7.9 FSW $-18k, but current spending is much more than left in budget