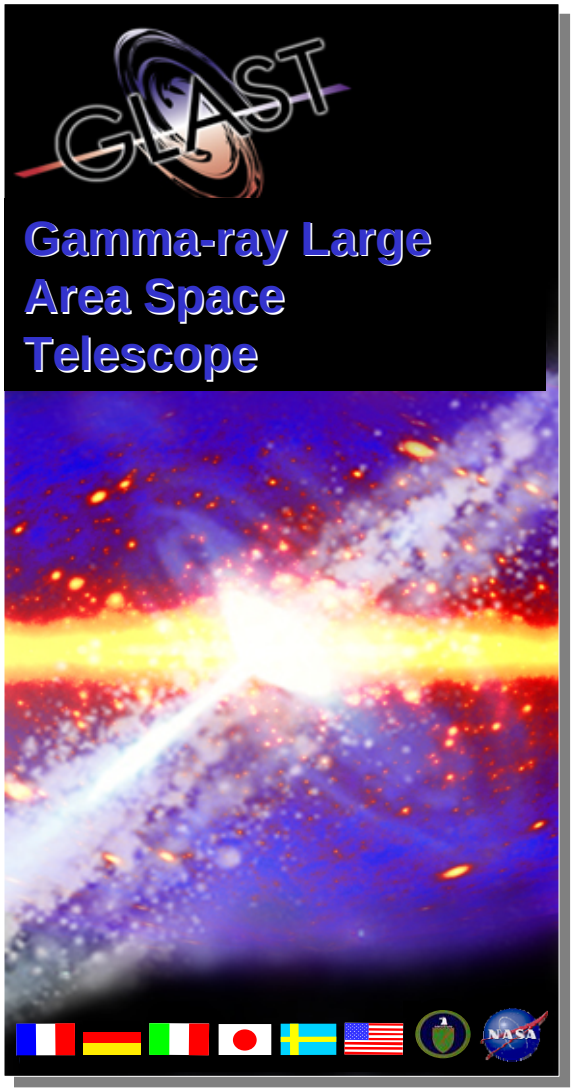


GLAST Large Area Telescope

LAT Reboot Resolution Team

Monthly Status

11/30/2006

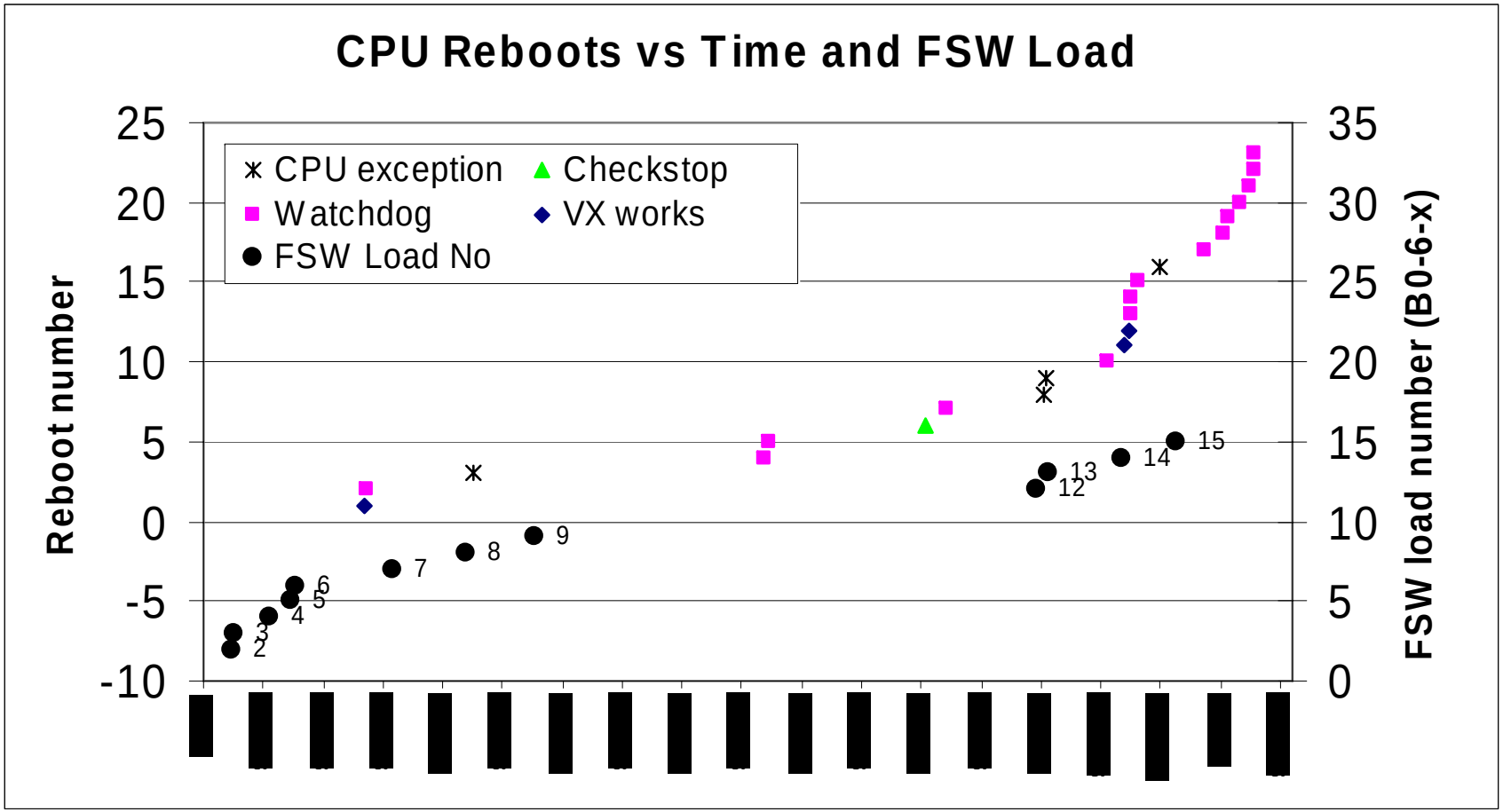
Erik Andrews
Jana Thayer

Tasks

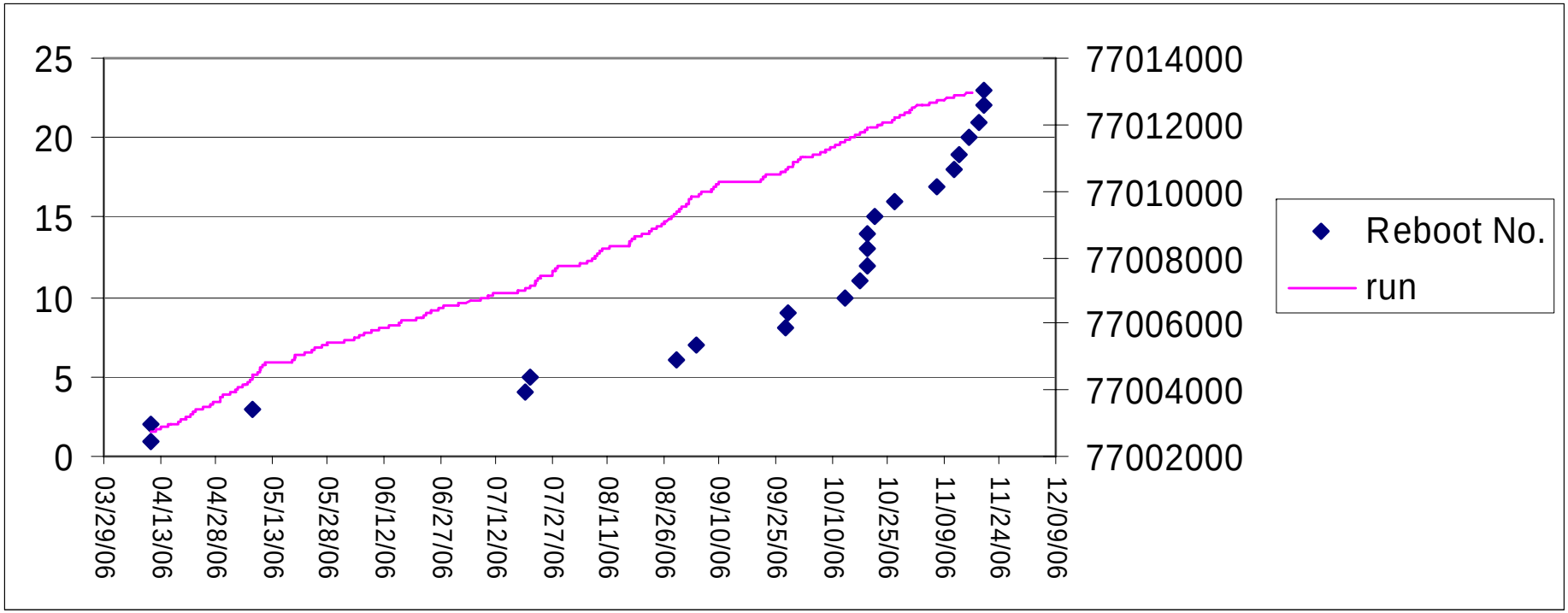
- **The tasks are focused in four primary domains:**
  - **A fishbone analysis to systematically identify potential causes, rule out causes where possible and identify the most likely causes to prioritize the reboot investigations**
  - **Utilizing existing or to-be-developed tools, to diagnose the root cause in selected previously occurring reboots on the LAT Instrument, sufficient to close the existing NCRs.**
  - **Development of tools and/or adaptation of existing tools for the LAT environment (BAE RAD750 with VxWorks) which can be utilized in an offline manner to further analyze dumped memory regions.**
  - **Identify and implement capabilities (and schedule estimates) for both transient (RAM) and/or the LAT FSW in EEPROM changes which could provide additional insight and detection of failures within the run-time system.**

- **Collaboration web site:**
  - **https://confluence.slac.stanford.edu/display/ISOC/FSW**

Reboots vs. Time & FSW Version



CPU Reboots vs. Time and Run Number



Instrument FSW Configuration (11/29 - 6pm AZ)

- **Build 0.7.0: Successfully Loaded 11/29**

- **Build 0.6.15: Loaded 10/31**
  - **LSW 0.1.1 (added Monday 11/20)**
    - **Added to flush cache to memory**
  - **Maximum Bank Time Field (set to 0x00) via LMEMLOADMEM (added Tuesday 11/21)**
- **Recent Reboot History:**
  - **Baseline 0.6.15: 7 in 21 days**
  - **0.6.15 Plus LSW 0.1.1: 0 in 2 days**
  - **0.6.15 Plus LSW 0.1.1 + Timer Disable: 0 in 1 day**
    - **** Statistically insignificant time durations ****

Fishbone Analysis (1/2)

Cause	Discussion	Status
1 Hardware failure induces reboot		
1.1 Component failure		
1.1.1 Isolated part failure	Reboots seen on all processor, so it cannot be an isolated part failure.	Eliminated
1.1.2 Design defect causes stresses that take out specific parts systematically	Lower level architecture reviewed. Very unlikely that a design error would stress components on the SIB or LCB that could cause reboots but otherwise operate normally. BAE stated no similar reboots on other programs	Very unlikely
1.1.2.1 CPU board		Very unlikely
1.1.2.1.1 Bridge chip		Very unlikely
1.1.2.2 SIB		Very unlikely
1.1.2.3 LCB		Very unlikely
1.2 Environmentally induced		
1.2.1 Vibration failure damages chips	Issue documented in NCR 803 and 833. All boards inspected with no sign of damage.	Eliminated
2 Software induced reboot		Possible
2.1 Operating system flaw		
2.1.1 Priority inversion	Code has been designed to avoid this issue	Unlikely
2.2 Application software bug		
2.2.1 Memory overwrite	FSW-823, FSW-831	Possible
2.2.2 Interrupt locks	Code has been designed to avoid this issue	Unlikely
2.2.3 Task death	Would expect to see side effects or exceptions	Unlikely
2.3 Boot level		
2.3.1 Boot I/O		
2.3.2 Interfaces/contention		

Fishbone Analysis (2/2)

1. Cause	Discussion	Status
2.		
3. Operations/environment		
3.1. Over/undervoltages	Review of telemetry showed no sign of over or undervoltage	unlikely
3.2. Command sequence has unintended side effects	Reboots have occurred with no active commanding to EPUs or SIUs. Background transactions from VSC are covered in 3.3.	Eliminated
3.3. VSC induced	General note: LAT has been designed to be robust in the face of erroneous or unexpected data from the spacecraft/VSC.	
3.3.1. Erroneous times in timetones induces reboots	Detailed review of data from Nov 1 to Nov 16 showed no unexpected values in timetone messages. During this interval there were numerous reboots. Single instances of a reboot still could have been caused by bad values in timetone messages.	Very unlikely
4. LAT software interacts with computer firmware/operating system feature		
4.1. Feature documented in vendor errata sheets	General note: examined errata from vendor, including newly disclosed features.	
4.1.1. Errata 13	Workaround already implemented	Eliminated
4.1.2. Errata 15	LAT is susceptible, documented in FSW-820, FSW-821	Possible
4.1.3. Errata 20	Alternate workaround already implemented	Eliminated
4.1.4. Errata 24	LAT is susceptible, documented in FSW-822	Possible
4.2. Undocumented and previously unknown errata		
4.3. 1553 I/O issues		
4.4. Interrupt handlers (PPS, GRB)		
4.5. cPCI bus contention		

Diagnose/Document Root Cause of Past Reboots

- **Accomplishments**
  - **Leveraging off previous analysis by LAT FSW & Systems team**
    - **Identifying any additional paths to follow.**
    - **Believe there to be fairly low probability of success with most – primarily due to the dumped data content is very limited until the most recent few.**
      - **For these most recent few, anticipate attempting to use off-line tools once ready.**
  - **Telemetry Content**
    - **Analysis of relevant time period around reboot for clues in hkp and diagnostic telemetry packets**
  - **Other context information**
    - **VSC state (health, context)**
    - **Message logs from run with LAT activity and timeline**

- **Plans**
  - **Past Reboot Report Summary and recommended closure path for related NCRs.**

Off-line / Post Mortem Tools

- Accomplishments
  - The team has identified memory regions which should be dumped when a reboot occurs.
    - Provided to Operations in formalized procedures
    - Other procedures to periodically characterize the running system have been identified, checked out, and provided to Operations
  - Adapting capabilities from Wind River provided with VxWorks for 750.
    - Tools provided by the NRL were fairly heavily tied to their MIPS processor architecture (not surprising).
    - Will utilize NRL SIU and/or test systems at SLAC (remotely) to test and verify the P-M tools as they come on-line.
  - Capabilities In work
    - Unwind Stack – Interpreting the Stack Traces with gdb/crosswind. Attempt to utilize the existing code to support this. If successful, should have something by mid-December.
    - Analyze PC, TCBs – Next on the list after the stack trace
    - Check for memory overwrite conditions
- Plans
  - Initial capabilities to trace back the stack to be completed mid-December.
  - Additional capabilities (TCB analysis, memory analysis) to be completed after the stack trace tools.

In-line Diagnostics / Instrumentation / Bug Fixes

- **Accomplishments:**
  - **LSW: Writes Task, Time, Priority and PC to the ring buffer.**
    - **LSW 0.1.1 flushes its information from the cache out to RAM so it is available for dumping if reset occurs.**
  - **Code Validation**
    - **IVV exercising their tool suite (InSpect, Flex-elint) on build 0.7.0 – focused on memory manipulation and potential memory over-write or alloc/dealloc deficiencies.**
  - **Interrupt Locks**
    - **Desk checked verification for correct utilization**
    - **Initial investigation of instrumenting these has been done**
      - **Potentially significant performance impact.**
- **Plans**
  - **LSW Enhancement: Stack Pointer and WD timer value (~ 2 weeks) (JIRA #829)**
  - **IVV to report out by December 15 on their findings.**

Code Enhancements

- Accomplishments / Process:
  - All RRT recommended changes to FSW are being tracked in the JIRA system
    - Means Project approval for each/all
  - Errata Related
    - Erratum #15: Simultaneous Snoop with CPU Read Hang (JIRA #822, #824*, #832*) * = Clones in SIU/EPU boot code. Deferred.
    - Erratum #24: Memory Controller Max Bank Active Timeout Hang (#820, #821, #823)
  - Desk Checking key sections of the code
    - Potential LRA cmd/resp lists processing conflict with #15 (# 826)
    - Identified & recommended changes to LPA (#831)
- Plans
  - Add to the LSW: Stack Pointer and WD timer value (~2 weeks)
    - Additional capabilities to be worked when these complete. (#829)
  - Incorporate changes based on JIRA items above into next builds of the FSW.
- Issue (of Coordination)
  - Stand down for installation of LAT on the Observatory

DAQ Test Bed

- Accomplishments
  - Arranged for extended periods of testing / availability
    - Friday thru Monday for December
    - Other times as necessary to test / checkout additional capabilities or concepts

- Plans
  - Develop mechanism to feed data from science/muon runs on the instrument back thru the FES into the testbed. Jana working with Ric, Owen, Gregg to implement.
    - Seeking to duplicate data types and rates into the DAQ as seen on the instrument.
  - Non-trivial activity to get the testbed close to the Instrument environment.
  - Flight spare/qual crates and GASU
    - Develop plan to place these units on the test-bed to reproduce the reboot phenomena.
    - Includes giving the two units identity and current code baseline
    - Available for 'next step' if work on test-bed doesn't show reboots happening during extended testing with EM crates.

RRT Schedule – Upcoming Activities/Milestones

- 11/29 - Build 0.7.0
- 12/1 – First Iteration of Fishbone. Determine actions for next levels of investigations.
- *12/6 – Install LAT on SC (?)*
- 12/8 – First cut at P-M tool to trace back the stack.
- 12/8 – Fishbone Analysis report out. Determine next steps here.
- 12/13 – Review draft of early reset closure path
- 12/14 – Build 0.7.1 (tbr)
  - Include JIRAs from RRT recommendations (and others previously worked)
- 12/15 – IVV Report back on static analysis
- 12/20 – Report on initial use of testbed for 3 extended runs (4-day weekends)
- 2007 - longer term LSW enhancements
- 2007 – Build 1.0.0 - GRB Algorithm incorporated