

Monthly Status Review

LAT Testbed Status

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Gregg Thayer, jgt@slac.stanford.edu
Stanford Linear Accelerator Center

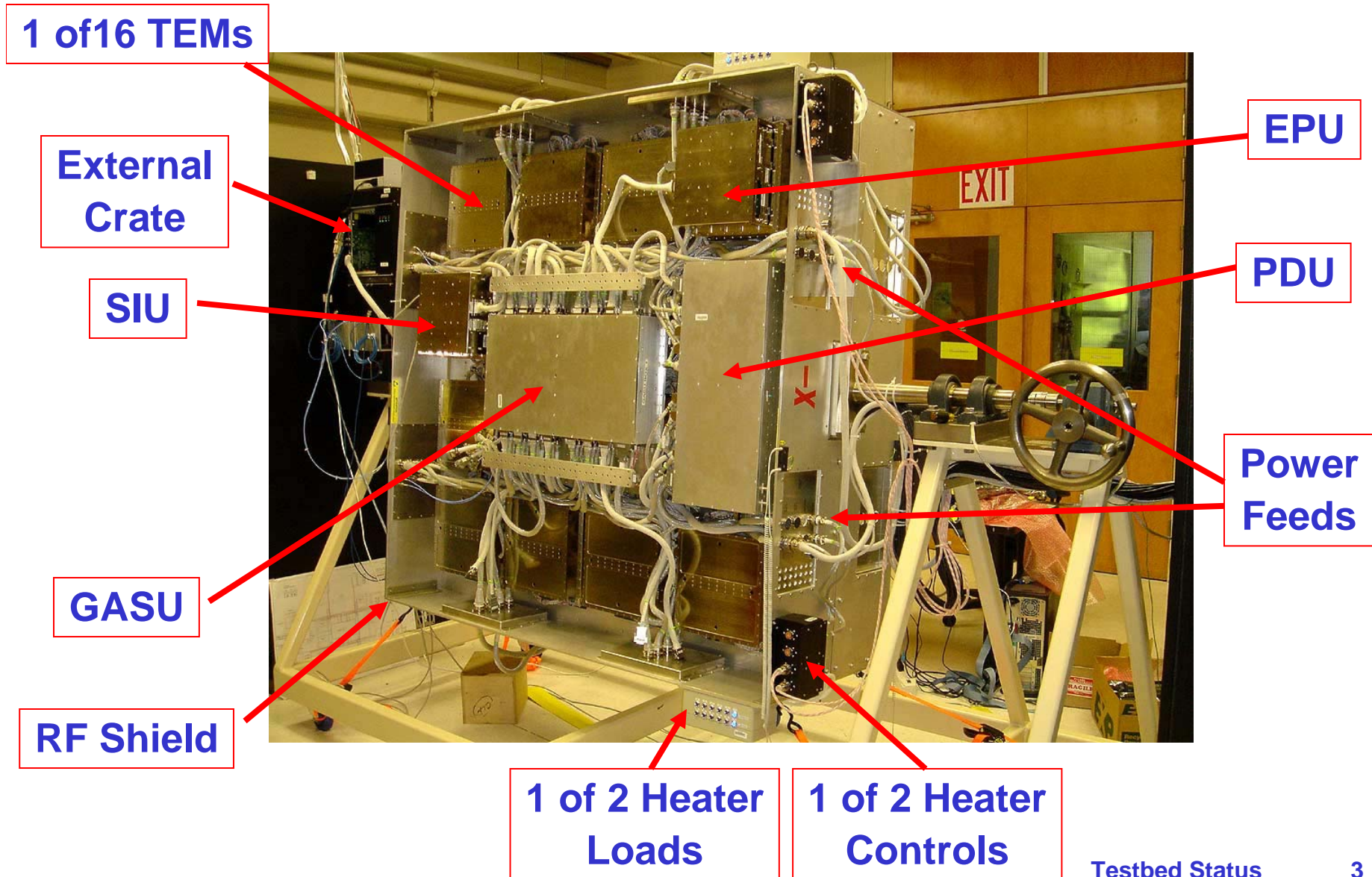


Overview

- The Testbed is a complete “flight-like” Trigger and Dataflow system with simulated front-end inputs.
- Purpose of the Testbed
 - Validate the Level 3 Filter
 - Validate Flight Software
 - Validate Trigger and Dataflow System
 - Eventually, passed to ISOC
 - Can be used to test on orbit scenarios
- The testbed is the *only* place where all parts of the T&DF system are assembled in a test environment
 - The last line of defense for catching system-level problems



The LAT Testbed (-z)

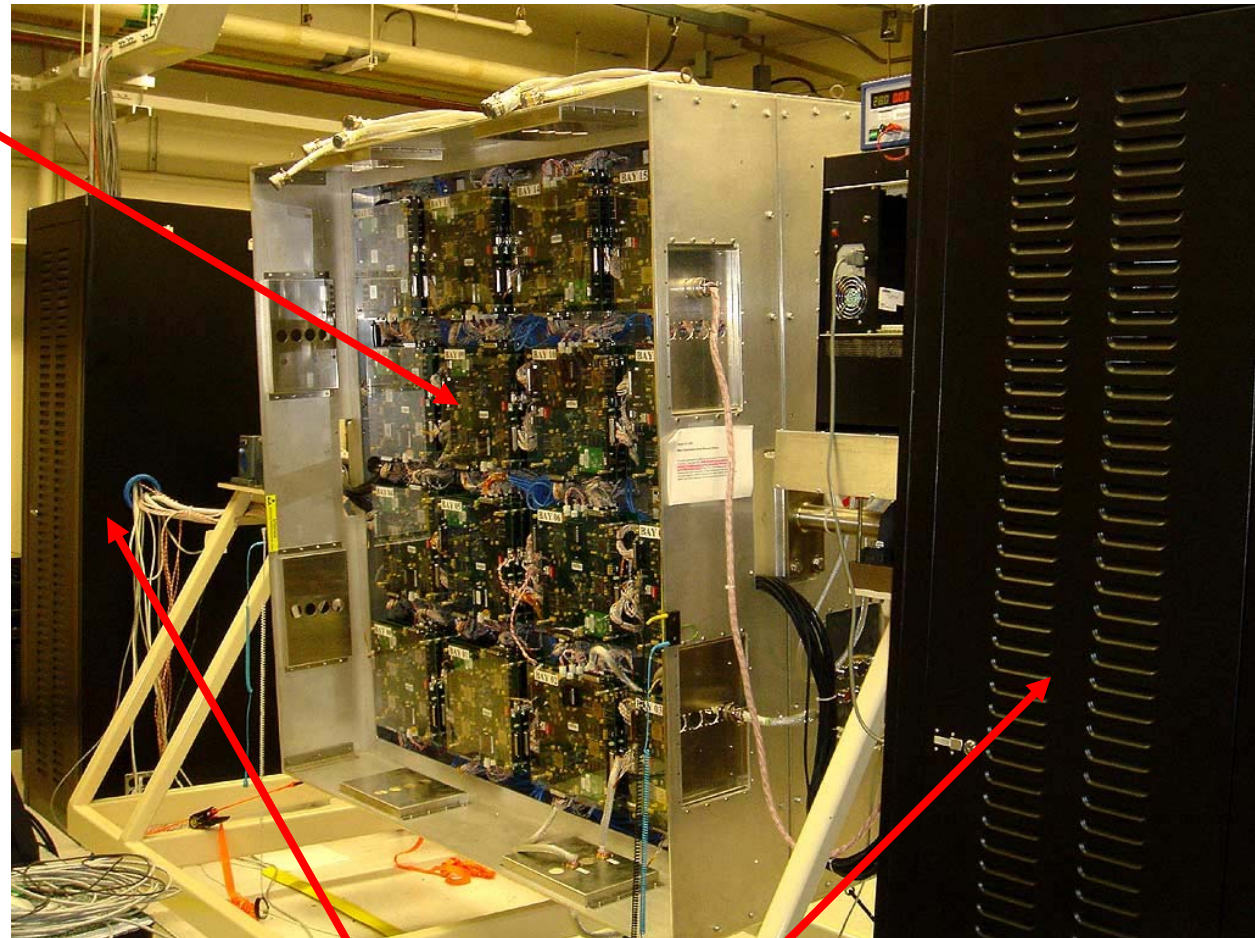




The LAT Testbed (+z)

16 TKR FES
16 CAL FES
8 ACD FES
1 Control FES

16 Tower Loads

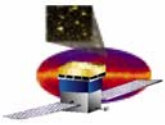


11 FES Control PCs



Hardware Status

| Component | Need | Have | Status |
|--------------|-----------------------------|----------------------------|--|
| TEM | 16 Updated | 6 Updated 10 un-updated | 4 Updated, awaiting testing 6 Awaiting update |
| SIU | 2 | 1 | Cold Spares to remain unpopulated (due to limited BAE Boards) |
| EPU | 3 | 2 | |
| GASU | 1 | 1 | To be upgraded |
| PDU | 1 | 1 | To be upgraded |
| FES | 41 FES Boards | All | Functionality Verified |
| Tower Loads | 16 | All | Functionality Verified |
| T&DF Harness | 121 cables, 20 varieties | All | Complete and verified |
| FES Harness | 192 FES-TEM 24 FES-AEM | All FES-TEM 3 FES-TEM | 21 FES-TEM cables queued, pending arrival of connectors |



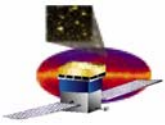
Schedule

- TEM upgrade to be completed in conjunction with PDU and GASU upgrades
- A sample of ACD-FES have been checked for length and connectivity, assembly of remainder is queued
- As hardware is upgraded
 - Critical to re-verify connectivity and data-path
 - FES → TEM → GASU → EPU/SIU/LATTE
 - Example: Use FES to tickle every trigger line in all 16 TEM every time a TEM is replaced.
 - More extensive regression test suite is desirable
 - Get this for free as a product of developing FES with the goal of testing the Level 3 Filter



Front-End Simulators

- New collaborators from *The* Ohio State University
- Developing a architecture for generating and processing simulated input
 - Creating FES input
 - Diagnostic Samples (trace-back)
 - GLEAM MC Samples
 - Organizing and moving the large files
 - Controlling the timing of the FES signals to T&DF
- This will allow comprehensive testing of the trigger system, data integrity and flow, as well as regression tests to verify low level connectivity
- Weekly (nominally) meeting to coordinate effort



Summary

- The LAT Testbed is the only place to verify the T&DF system in a test environment
- Testbed hardware to be fully upgraded in next few weeks
- The system is complete and has already proved itself useful as the only multi-tower teststand.
 - Example: A bug was discovered in the FPGA code that accounted for the relative rotation of the TEMs in odd numbered bays.
- Our priorities:
 - Test a vertical slice of the data path in the next week to continue the bootstrap process of debugging the FES and T&DF system
 - Continue to develop the tools to comprehensively test T&DF