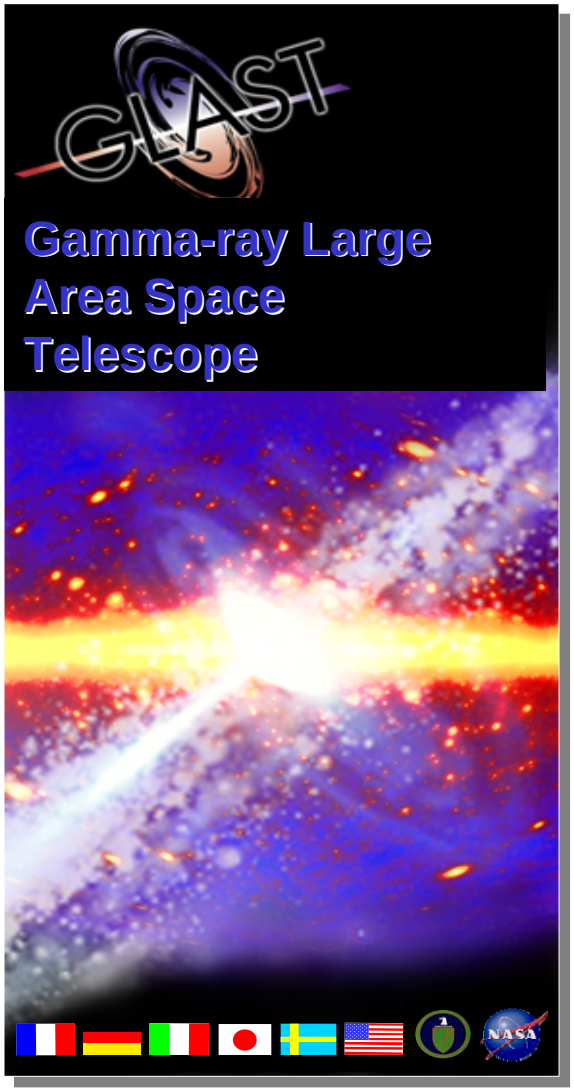

GLAST Large Area Telescope

Systems Engineering

Test Status, NCRs and Verification Status

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LAT Test Status

- **FSW upload/regression test**
  - **FSW regression testing completed successfully**
- **CPT Status**
  - **Completed over the weekend**
  - **ACD power up (charts follow)**
  - **Two orbit test**
    - **Hampered by adapting to B1.0.1 and operator errors**
  - **Timing test**
    - **A side demonstrated performance with GPS locked and unlocked (combining both runs)**
    - **B side not demonstrated successfully**

CPT Flag Status

- 29 flags were LAT related
  - 6 for one time executions
  - 2 for commanding issues
  - 3 for side effects of fast clock due to SC configuration (including ACD FREE power up)
  - 3 for operator errors
  - 9 for script/config errors
  - 3 to change order of operations or repeat tests
  - 2 for unexpected VCHP feed state
- 7 of the 29 are closed as of GD status sheet dated 7/30
- No significant LAT flags that would hold completion of the CPT
- One of the commanding errors was a dropped command, always a concern

Problem w/ Configuration 3 ACD power up

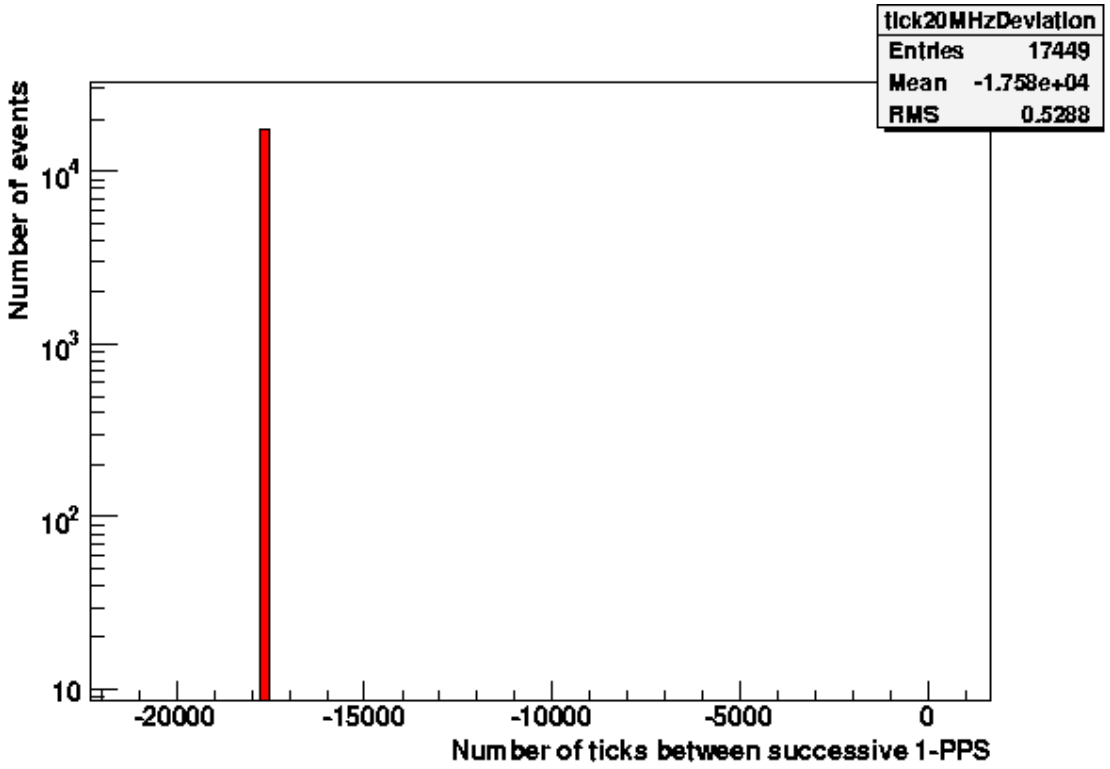
- On 7/27/07, during power up in Configuration 3, the ACD 3.3V current was above the limit
  - Additional veto drivers on all FREEs were enabled (a benign state)
  - This is the default power up state of the FREE boards. During the power up sequence, FSW explicitly disables both veto drivers.
- Why were the veto drivers left enabled?
  - FSW power up sequence:
    1. ACD FREE card is powered (both veto drivers enabled)
    2. Delay one second
       - 1 sec based on CPU clock ticks calibrated to PPS sent by SC
       - The purpose of this delay is to wait for the 1 sec burst of low frequency clock ticks sent by the GASU to the FREE during power up initialization.
         - The duration of this burst is set by the frequency of the LAT clock (40 million ticks of the LAT clock oscillator)
    3. Look-at-me command is sent to FREE to set up the communications fabric
    4. Register on FREE is written to disable both sets of veto drivers
  - Silence of the LAMs: if the LAM is sent to the FREE before the 1 sec burst from the GASU has ended, it is ignored by the FREE

Problem w/ Config 3 ACD power up (2)

- LRA was used to issue LAM to FREE boards and continue with CPT in configuration 3 while the problem was debugged offline
- Source of the problem was an ~880 ppm shift in the UDL PPS output period, possibly related to the sequence of commands issued to revert to normal operations at the end of the "unlocked" muon telescope run.
  - To "unlock" the GPS, GD switched the UDL into ground override mode
    - If GD disabled the Viceroy while the UDL was still in manual override, then some bad samples of the Viceroy PPS period may be used to seed the input of the 100-second averaging computation prior to the deassertion of GPS_VALID
    - After manual override is disabled, the UDL reverts to using the 100-second average (because the Viceroy is already inactive) and the average is skewed because of the bad samples.
  - The error is probably procedural: The Viceroy was shut down before disabling the ground override rather than after
- The ACD power up problem was duplicated on the Testbed by artificially decreasing PPS period
- FSW-967 created to increase delay between the power up and the LAM in FSW from 1.0 sec to 1.5 sec in order to take into account the maximum variations in the PPS clock and in the LAT clock period over the course of its lifetime
  - Pending approval by project CCB

Problem w/ Config 3 ACD power up (3)

- **Evidence for 880 ppm shift in PPS:**
  - **LAT counts and records the number of ticks of its 20 MHz clock between successive PPS pulses**
    - **The PPS pulse is short by 17,580 ticks or ~880 μs**



NCR Summary Status

Closure Plan	Definition	Count
Work continuing		
QAR	CND or other issue transferred to a QAR	9

LAT Level Verification Status

Category	Verification Method					Totals	
	Test	Demo	Analysis	Inspection	Children		
	# Comp	# Comp	# Comp	# Comp	# Comp	Complete	% Comp
Requirement Identified	121	73	206	37	21	458	100.0%
Flow Down Complete	121	73	206	37	21	458	100.0%
Draft Verification Plans	121	73	206	37	21	458	100.0%
Final Verification Plans	121	73	206	37	21	458	100.0%
Verification Plans Executed	104	63	194	35	15	411	89.7%
Verification Reports Submitted	104	63	194	35	15	411	89.7%
Requirements Sold	104	63	193	35	15	410	89.5%
Expect Compliance	0	0	0	0	0	0	0.0%
Verifications Plan Deferred	17	10	12	2	6	47	10.3%
Requirements Issues	0	0	0	0	0	0	0.0%
Total VPs	121	73	206	37	21	458	

- **Progress this month**
  - All 458 VPs are Final
  - 410 of 411 VPs planned for execution have been approved by GSFC
    - 1 VP conditionally approved pending release of the EMI Test Report
    - 1 SRD VP (Background Rejection) in work by GSFC
- **Status**
  - VCRM version 27 released
  - All deferred GRB reqts will be sold post FSW B1.0 installation