GLAST Large Area Telescope:
Planning Meeting
December 10, 2003
AntiCoincidence Detector (ACD) Subsystem
WBS: 4.1.6

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Outline

- Near-Term Milestones
- Recent Progress
- Interdependencies
- Open design issues
- Issues/concerns/suggestions/risk

Near Term Milestones - updates

Milestone Description	Date	New Date	Status/Notes
Base Frame Channel Fabrication start		9/20/03	*Due 12/15/03. Two weeks late due to electroless nickel addition. Due 1/5/03*
Complete Fab of TDA tiedowns	August	12/15/03	*In fabrication/on schedule. Delayed by interference fixes*
Receive/Test Flight ASICs (rapid-package)	Sept./Oct.	11/30/03	*LATE. What is new date? 12/23? ASICs received 10/2/03. Testing in progress*
Start Fab Flight HVBS PCBs	August	12/5/03	*Minor change following review. Design additions being made, submit for fab before Christmas*
Complete Flight Mechanical Drawings	September	12/31/03	*Delayed by interference fixes. Receiving additional engineering and design support to complete.*
Complete Design on MGSE and EGSE	October	12/31/03	*New designer working on MGSE*
Complete Assembly of Flight Shell	October	1/15/04	*Receive panels 11/28; delayed by interference fixes. First panel machined, remaining in process. Receive panels on 12/19. Flight shell assembly will slip out to early February*
Start Testing on BEA EU	November	11/20/03	*Assembly of electronics chassis started. Hardware being finished up PMT problems and GAFE selection delayed progress. Start 12/22 Assembly in process*
Complete Fab of Clear Fiber Cables	August	1/15/04	*Connectors complete; work started on assembly. Problem during assembly, fibers damaged by cleaning process. Estimate 2-3 week delay*
System Test w/ two FREE Boards, HVBS, PMTs and TDAs		11/28/03	*Preliminary test Sept,*
Complete Fab of Flight TDAs	November	1/15/04	Flight TDAss successfully wrapped and light tight tested. Recieving first shipmnet on 12/23
Complete PMT Assembly	January, 2004	3/30/04	*Need to resolve some workmanship issues before full production. Workmanship issues addressed, resuming assembly of 5 non-flight PMTs. PMT failed during thermal testing.*

Recent Accomplishments

- **Tile Detector Assembly**
  - 65 of 89 TDA Assembly drawings complete
  - 85 of 89 Tile drawings complete
  - First set of flight TDA's successfully wrapped and light tight tested
  - 82 tiles machined and polished, 44 TDA's assembled, 10 fully wrapped
  - Will receive 20 TDA's from Fermi on 12/23
- **FREE Boards**
  - Assembled FREE ETU using rapid packaged flight ASICs. Flight tooling and process verified. Currently being tested. Update: finished this morning and beginning installation into chassis.
  - FREE PCB design complete and out for bid. Vender selection this week. Update: Vender selected
  - Parts being prepared for flight assembly
- **Clear Fiber Cables**
  - All machined parts completed
  - Fibers cut to length and cleaned. These fibers were damaged by cleaning. More fibers being cut to length using spare material. Additional fibers ordered to replace damaged material.
  - Fiber connector gluing fixture designed and fabricated
  - Stuffing fibers in connectors. Begin gluing this week.

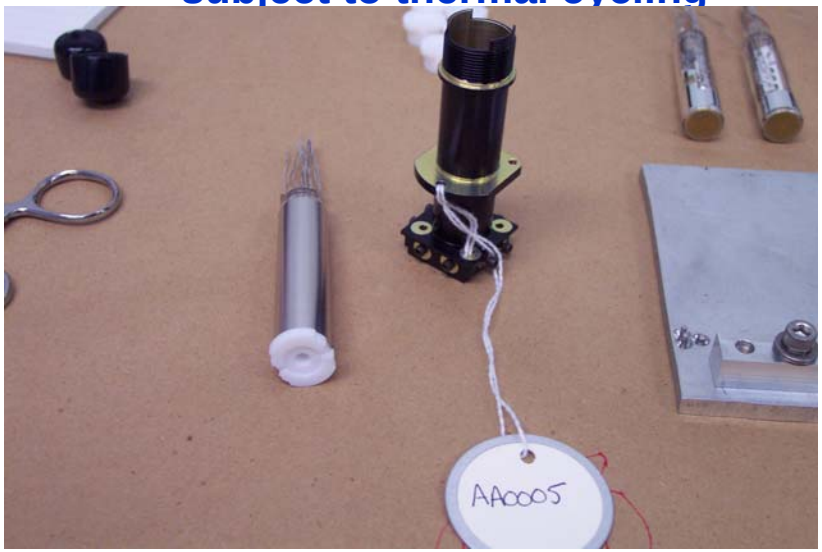
Recent Accomplishments

- Shell Panels
  - Successfully completed machining of one panel
  - Remaining panels in machining
  - Will receive completed panels on 12/19
- ASICs
  - Prepared to test ASICs upon receiving them
  - Performed SEU testing on ASICs at TAMU, more later
  - Radiation testing at Brookhaven in January? Can ACD piggyback on this testing? Dates?
- Base Frame
  - EO for electroless nickel completed. Delays channels by 2 weeks. New due date 1/5
- Schedule Review held on December 9
  - 5 hour review with members of upper management
  - Final result, schedule is difficult but possible

Recent Accomplishments - Photomultiplier Tube (PMT) Assembly

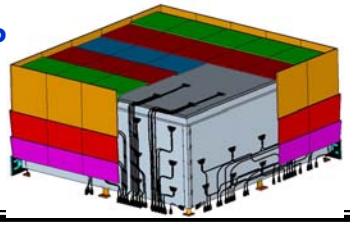
- **PMT Assembly Effort**
  - ✓ **18 EU PMTs have been assembled**
  - ✓ **5 were subjected to thermal vacuum testing**
  - ✓ **1 failed testing at -30C. Glass seal broke.**
  - ✓ **All others performed fine**
  - ✓ **Investigation underway to determine root cause of failure**
  - ✓ **Remainder of Qualification PMTs will be subject to thermal cycling**

PMT Bonded in mechanical housing



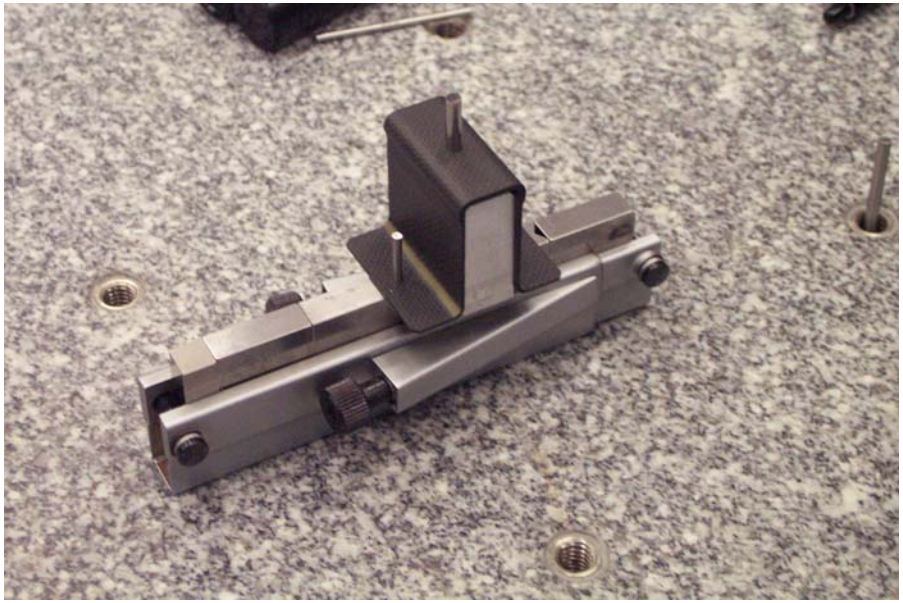
Preparing for PMT bonding

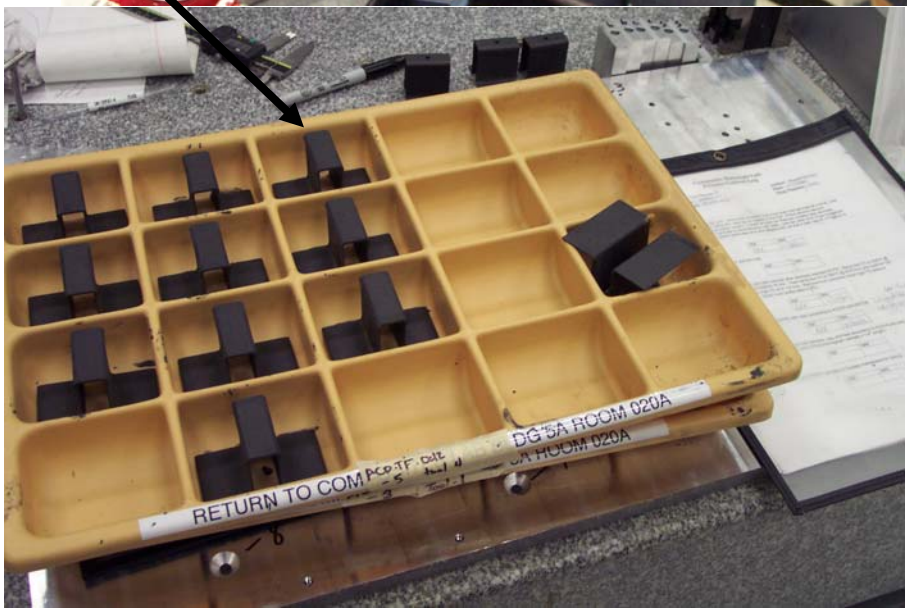
- **Workmanship Problems have been addressed**
- **Adding more experienced technicians and QA to the assembly team**
- **May move into a new facility**
- **Assembling 5 more Engineering Units this week to verify corrective action will resolve workmanship problems**

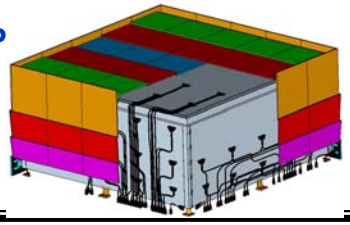


TDA Flexures

- **Tile Flexure Fabrication In Progress:**
  - **Flexure Blanks Made**
  - **Individual Flexures Cut**
  - **Flexures Inspected on Go- No Go Gauge**

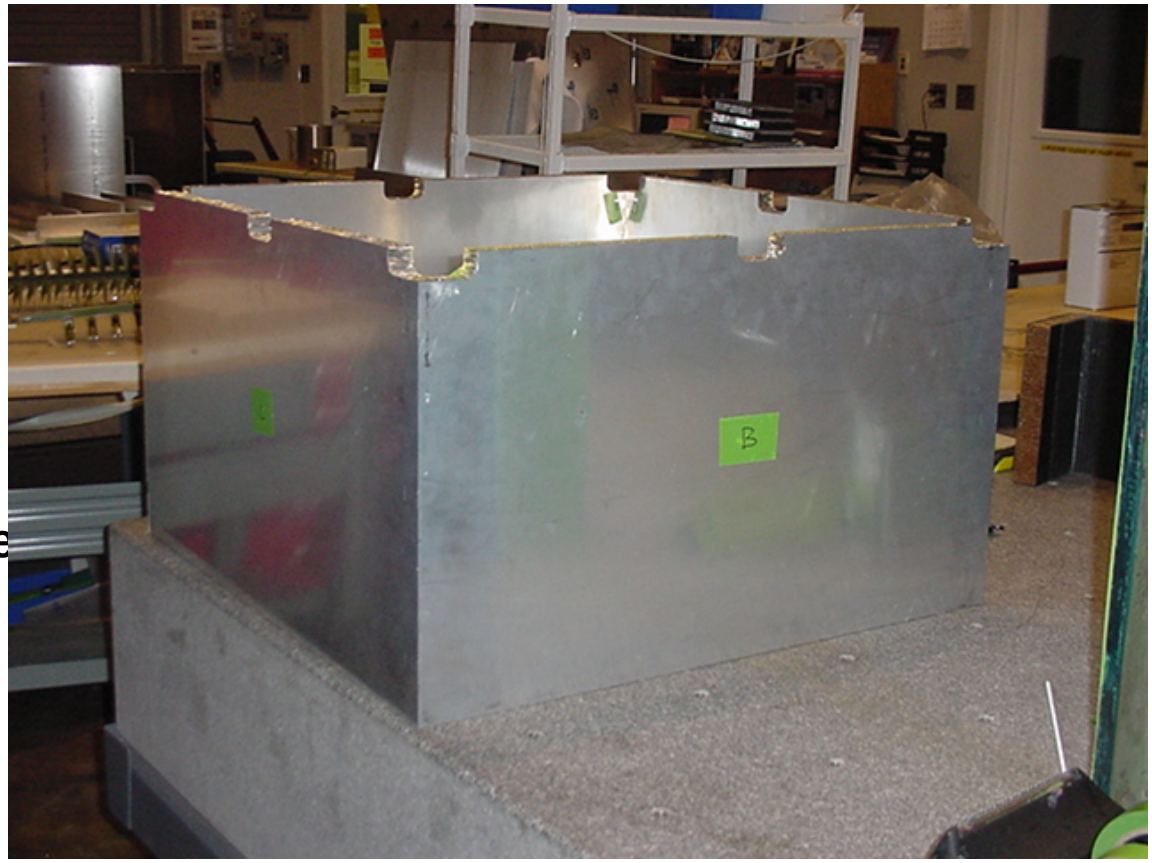






ACD Mechanical Status - TSA Process Development

- **TSA Shell Assembly Development**
  - ✓ **½ Scale TSA being worked for Bond Process Development Effort**
    - ✓ **Panel to Panel Bonding Procedure Drafted, Ready to Implement**



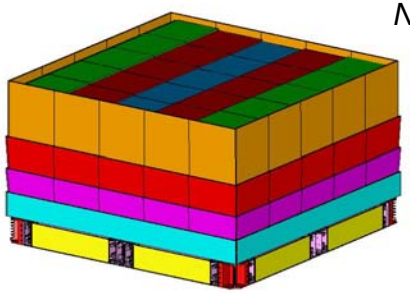
½ SCALE ACD SHELL ASSEMBLY – BEING ASSEMBLED TOP SIDE DOWN

FABRICATION, ASSEMBLY AND TESTING STATUS

Number needed in parenthesis

STATUS KEY

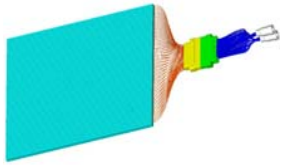
- Prototyped
- In Fabrication or Ordered
- Received
- In assembly
- Assembled
- Tested



ACD Assembly (1)

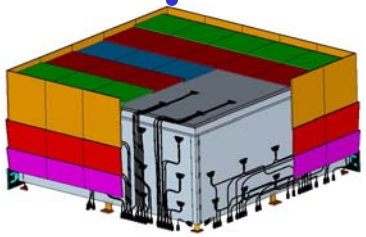
6
130

Clear fiber cables (130)

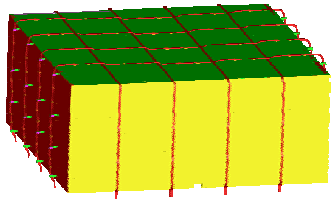


12
77

Detector assemblies - TDA - (4 basic types, 89 needed total)

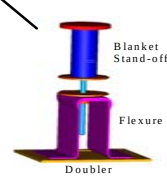


Tile Shell Assembly –TSA (1)



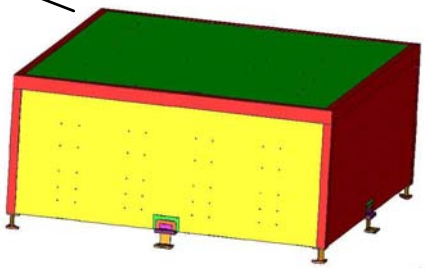
1
8

Fiber ribbon detectors (8)



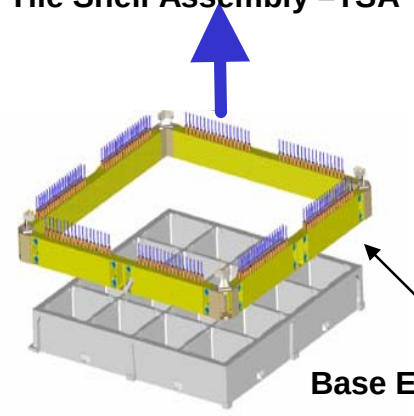
8
386

Detector Flexures (366+20 spares)



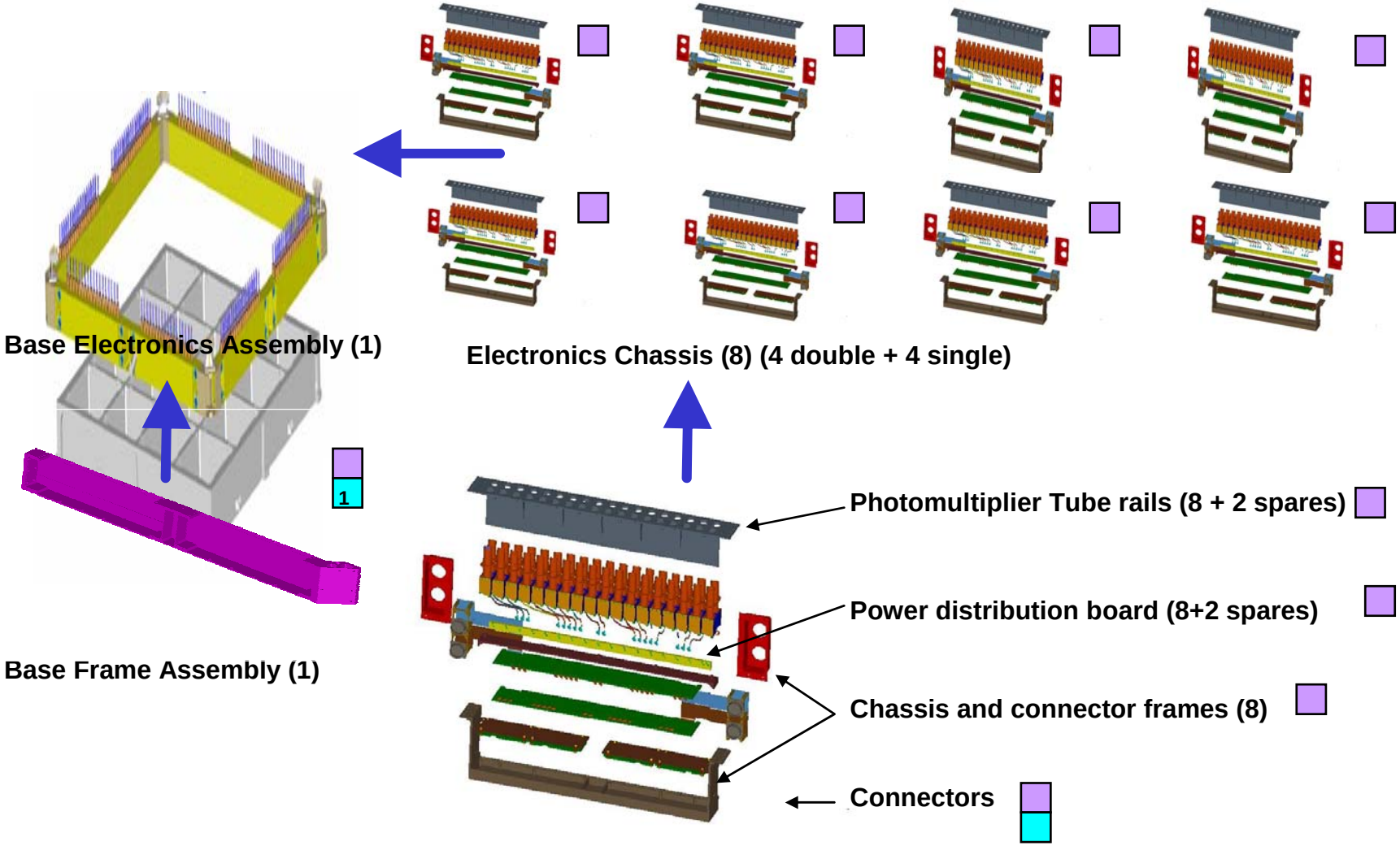
1

Composite Shell Assembly (1)



Base Electronics Assembly (BEA) From next page

FABRICATION, ASSEMBLY AND TESTING STATUS



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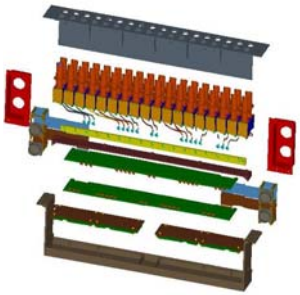


Electronics Chassis (8)

(4 double + 4 single)

Electronic Chassis Subassembly Item	Needed	Proto	Assembled or received	Tested	Ready for higher assembly
Photomultiplier Tube Assemblies	194 + 46 spares	Yes			
Photomultiplier Tube (PMT)	194 + 46 spares	Yes	240	240	230
Photomultiplier Tube housings	194 + 46 spares	Yes	240		240
Photomultiplier Tube resistor networks	194 + 46 spares	Yes	All PCB's & parts		
Front End Electronics (FREE) 'right hand' boards	*8 + 2 spares*	Yes			
Front End Electronics (FREE) 'left hand' boards	*4 + 2 spares*	Yes			
GLAST ACD Front End chip – GAFE	*194 needed, 650 ordered*	Yes			
GLAST ACD Readout Controller chip – GARC	*12 needed, 125 ordered*	Yes			
Digital to Analog Converter - DAC MAX 5121	24 + spares	Yes			
Analog to Digital Converter – ADC MAX 145	194 + spares	Yes			
High Voltage Bias Supplies (HVBS) boards (24 + 6 spares)	24 + 6 spares	Yes			
High Voltage Capacitors (218 + 52 spares)	218 + 52 spares	Yes	270 (replacment)		

Interdependencies

1. Delivery of FREE Boards and ASICs to Electronics for test bed. – late January/early February
2. EGSE/G3 – Ongoing development with I&T and Electronics groups. Have not received G3 software (due in October) so that we can begin mitigating late delivery of EGSE/G3. Prototype power supply delivery date? Updated delivery date for limited G3 and full G3? Could we get another limited version of the G3? G3 availability is a bottleneck for testing.
3. ACD/GASU – Cable details and system clock testing. Need signed off and configuration controlled drawing for cables.
4. Grid to Base Frame match drilling – Outline drawing and available date for work? First window of opportunity in early February, next date in mid March, final date at ACD to LAT integration. ACD model delivered, still having problems with it?
5. Delivery of ACD Calibration Unit or subset to LAT I&T – working details for a February delivery.
6. ASICs – Delivery date?

Open Design Issues - update

- OPEN: Outline drawing that defines some interfaces with LAT is still not complete (blanket attachment, grounding, cable tie-downs, optical survey mounts). Action Plan: Work with LAT mechanical design team to resolve open issues. Status: Mechanicals are iterating 3D models.
- OPEN: Need updated interface loads following Grid design changes. Action Plan: Review ACD analysis when updated loads are received. ACD will not delay fabrication of mechanical components due to this open issue (slight risk in doing so). Status: Received new loads from Goddard this week.
- OPEN: Interference between some waveshifting fibers and TDA flexures. Action Plan: Re-design and re-analyze to resolve. Status: Working on finalizing lower tile flexures
- OPEN: Configuration change on BEA connectors requested by ACD; requires re-routing of some LAT cables.

  Status: Engineering presentation made; formal CR in process. Need to finalize cable routing

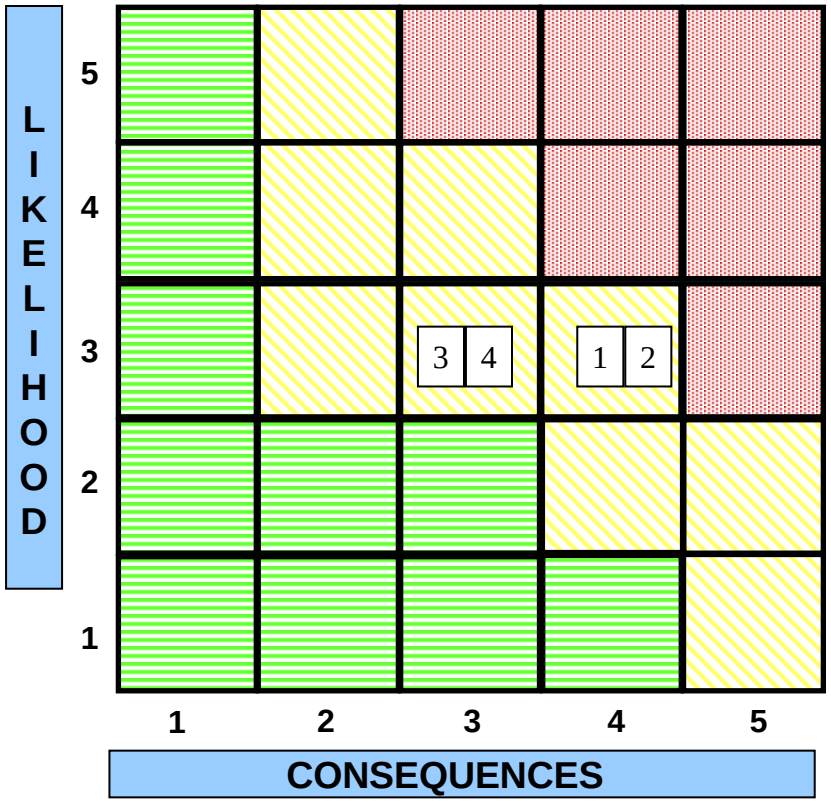
Issues and Concerns - Update

- Late delivery of G3 Test Stand/EGSE from LAT Electronics and I&T is a concern
  - Scheduled for August, recently slipped to January/February
  - Developing workarounds, using older G2 Test Stands and bench electronics. Interfaces are less like the flight interface, but should allow FREE card testing. G2 can test half a FREE card at one time.
  - Developing the G3 software before the arrival of the hardware, to minimize the startup delay once the G3 Test Stands arrive. Have not received transition software yet (due in October)
  - Will not impact assembly of ACD flight electronics. For Electronics Chassis testing, the G3s have been identified as a bottleneck due to parallel testing requirements.
  - Additional software support will be needed. Plan to have a meeting at GSFC in January with Online software developers.
- Slow response of GSFC procurement has been a concern
  - A Program Specialist, who tracks and expedites procurements and reports to the ACD, has been assigned and is already helping.
  - Hardware coming in! Has not caused a major impact yet, but has made life very difficult.

New Issues and Concerns

- **OPEN: ASIC Radiation Issue. STATUS: Waiting on report and data from GSFC Radiation Group. Plan on retesting GARC in January at Brookhaven? Or TAMU.**
- **OPEN: PMT Workmanship and Failure. STATUS: Workmanship issues addressed and are being worked. 5 more EU PMT's will be assembled this week. Working on determining root cause of PMT failure. Most probable causes of problem are mechanical mounting, soldering and manipulating the leads, or part defect.**

ACD RISK ASSESSMENT



Rank & Trend	Approach	Risk Title
1 →	M	Schedule/milestone slips
2 ↑	W/M	ASIC design and testing
3 →	M	Aggressive scheduling of E.M. tests and I&T due to schedule and cost pressure
4 →	M	Further cost growth

Criticality

High

Med

Low

Approach

M - Mitigate

W - Watch

A - Accept

R - Research

L x C Trend

↓ Decreasing (improving)

↑ Increasing (worsening)

→ Unchanged

GARC Parity Bit Problem

Discovered that one of the parity bits in the ACD data is unreliable under certain circumstances.

This bit affects the header of the ACD event data, which also contains the map of which tiles were hit. The error originated from a re-definition of the zero suppression bits between GARCv1 and GARCv2, carried over to GARCv3.

Under default operation, the parity bit behaves as expected. If a limit is placed on the number of PHA values to be read out, the parity bit becomes unreliable. The software being used to test the GARC was not checking this particular parity bit under these conditions. Other parity bits in the ACD data, including those for the PHA values, appear to be working as planned.

Even if we run the GARC under non-standard configuration, we have other cross-checks on the ACD data: comparison of the VETO map with the hit map, and comparison of both of these with the PHA values read out.

We will review ACD test procedures to be sure there are no other unchecked parameters.

LAT Electronics group is investigating other possible impacts.